International Conference on Ion Implantation Technology 2022

**Plenary Paper
* Invited Paper

SESSION MO1: Opening Session
Monday Morning, September 26, 2022
Presidential Ballroom, Second Level, Salons C&D

9:00 AM
Welcome and Overview - - Presented by Susan Felch, IIT 2022 Co-Chair

9:15 AM
In Memoriam - - Presented by Kevin Jones, International Committee Chair

SESSION MO2: Implant Systems
Monday Morning, September 26, 2022
Presidential Ballroom, Second Level, Salons C&D

9:30 AM MO2.01
Development of Ultra-High-Current Implanter for Material Modification Process in Next Era Devices
Hiroaki Kai; Nissin Ion Equipment CO., LTD., Japan

9:50 AM MO2.02
Particle Counts and Size Distributions after Implantation with On-Wafer Graphite Sources
Michael Current[1], Hideto Fujibuchi[2], Takahiko Ido[3] and Greg Lucchesi[4]; [1]Current Scientific, United States; [2]Ibiden, Ipswich, United States; [3]Ibiden, Ogaki, Japan; [4]II-VI Ion Implant Foundry, United States

10:10 AM MO2.03
High Temperature Electrostatic Chuck Enabled by BN Dielectrics Wei Fan; Momentive Technologies, United States

10:30 AM BREAK

SESSION MO3: Plenary Session I
Monday Morning, September 26, 2022
Presidential Ballroom, Second Level, Salons C&D

11:00 AM **MO3.01
Technical Developments of Thermal Annealing in the Past Sixty Years, and Future Perspectives Fred Roozeboom[1,2]; [1]University of Twente, Netherlands; [2]TNO - Holst Centre, Netherlands

11:40 AM **MO3.02
35 Years of Challenge and Innovation in Ion Implant
Tony Renau; Varian Semiconductor Equipment (retired), United States

SESSION MO4: Novel Doping Processes and Techniques
Monday Afternoon, September 26, 2022
Presidential Ballroom, Second Level, Salons C&D

2:00 PM *MO4.01
Smart Cut, FD-SOI and Integration Challenges
Didier Landru[1], Oleg Kononchuk[1], Nadia Ben Mohamed[1], Francois Rieutord[1] and Frederic Mazen[2]; [1]SOITEC, France; [2]CEA-LETI, France

2:30 PM MO4.02
Experiments and Modelling to Understand Implanted Layer Exchange Production of Isotopically Pure Si and Ge Layers for Quantum Computers Jonathan England and Ella Schneider; University of Surrey, United Kingdom

2:50 PM MO4.03
TEM Investigation of Extended Defects in Aluminum Implanted 4H-SiC Substrates Lydia Kuebler[1], Chappel Thornton[1], Hans J. Gossmann[2], Supakit Charnvanichborikarn[2], Christopher Hatem[2] and Kevin S. Jones[1]; [1]University of Florida, United States; [2]Applied Materials, Inc., United States

3:10 PM MO4.04
Comparison of Annealing Quality after 3e15/cm² 50keV BF_2^+ Implant Between Rapid Thermal Annealing and Furnace Annealing Leonhard Sturm-Rogon[1], Fuccio Cristiano[2], Karl Neumeier[1], Dirk Eckert[1], Ignaz Eisele[1] and Wilfried Lerch[1,3]; [1]Fraunhofer EMFT, Germany; [2]LAAS-CNRS, France; [3]Skylark. Solutions, Germany

3:30 PM MO4.05
The Examination of Source Life and Beam Parameters of Germanium Implantation Using Hydrogen Carrier Gas Weng Siong Chan, King Suen Lee, Henry R. Ignacio, Ching Chee Chu and James Huang; GlobalFoundries Inc., Singapore

3:50 PM BREAK

SESSION MO5: Novel Annealing Processes and Techniques
Monday Afternoon, September 26, 2022
Presidential Ballroom, Second Level, Salons C&D

4:20 PM *MO5.01
Where is the Annealing Technology Going for Better Device Performance ? Kyoichi Suguro; SUGSOL Corporation, Japan

4:50 PM MO5.02
Photoluminescence Characterization of He-Implanted SiC Upon Nanosecond Laser Thermal Annealing Elena Nieto Hernández[1,2,3], Gabriele Zanelli[1], Emilio Corte[1,2,3], Greta Andrini[2,3,4], Sviatoslav Ditalia Tchernij[1,2,3], Veronica Varzi[1,2,3], Federico Picollo[1,2,3], Ettore Bernardi[3], Ivo Pietro Degiovanni[3], Paolo Traina[3], Marco Genovese[3], Paolo Olivero[1,2,3] and Jacopo Forneris[1,2,3]; [1]Università degli Studi di Torino, Italy; [2]Istituto Nazionale di Fisica Nucleare, Italy; [3]Istituto Nazionale di Ricerca Metrologica, Italy; [4]Politecnico di Torino, Italy

5:10 PM MO5.03
Thermal Budget Reduction for Spike Anneals in a Conventional RTP Tool Silke Hamm, Rolf Bremensdorfer, Dieter Hezler, Alex Wansidler, Matthias Bauer and Christian Pfahler; Mattson Thermal Products GmbH, Germany

5:30 PM MO5.04
Nanosecond Pulsed Laser Activation of Phosphorus in Germanium Seunghun Baik, Heejae Jeong and Hyuk-Jun Kwon; Daegu Gyeongbuk Institute of Science & Technology, Korea (the Republic of)

SESSION TU1: Doping Applications
Tuesday Morning, September 27, 2022
Presidential Ballroom, Second Level, Salons C&D

9:00 AM *TU1.01
Laser Annealing Applications for Advanced FinFETs and Beyond Oleg Gluschenkov; IBM Research, United States

9:30 AM TU1.02
Ion Implantation Isolation for GaN HEMT: Mechanism and Parasitic Effects Hao Yu[1], Uthayasankaran Peralagu[1], Alireza Alian[1], Ming Zhao[1], Bertrand Parvais[1,2] and Nadine Collaert[1]; [1]imec, Belgium; [2]Vrije Universiteit Brussel, Belgium

9:50 AM TU1.03
Characterization of Structural Defects Induced by Heated Implantations and Annealing Process Pierre-Louis Julliard[1,2], Richard Monflier[2], Rémi Demoulin[2], Fuccio Cristiano[2], Sylvain Joblot[1] and Anne Hémeryck[2]; [1]STMicroelectronics, France; [2]LAAS-CNRS, France

10:10 AM *TU1.04
Ion Implantation Technology in SiC for Advanced Electron Devices Mitsuaki Kaneko and Tsunenobu Kimoto; Kyoto University, Japan

10:40 AM BREAK

SESSION TU2: Advanced Implant/Doping and Annealing Equipment
Tuesday Morning, September 27, 2022
Presidential Ballroom, Second Level, Salons C&D

11:10 AM TU2.01
Advanced Angle Control Requirements and Solutions for Enabling High Aspect Ratio Device Structures CheongIl Ryu[1], SeongSeok Choi[2], James S. DeLuca[2], Gary Cai[2] and Edward Eisner[2]; [1]SK Hynix, Korea (the Republic of); [2]Axcelis Technologies, United States

11:30 AM TU2.02
Precise Angle Control for Channeling in SS-UHE, Single Wafer Ultra-High Energy Ion Implanter Hiroyuki Kariya, Sho Kawatsu, Haruka Sasaki, Noriyasu Ido, Yasuhiko Kimura, Yoji Kawasaki and Mitsuaki Kabasawa; Sumitomo Heavy Industries Ion Technology Co., Ltd., Japan

11:50 AM TU2.03
PMOS Rc Reduction Using B_2H_6 Plasma Doping Process for Current and Next Gen DRAM Devices Vikram M. Bhosle, Jun Lee, Deven Raj, Toshihiko Miyashita, Chris Leavitt, Ilwoong Koo and Tim Miller; Applied Materials, Inc., United States

12:10 PM TU02.04
New ECR Ion Implanter with Advanced Temperature Control Sarko Cherekdjian; SHINE Technologies, LLC, United States

12:30 PM TU2.05
Introducing the Purion H200™, Single Wafer High Current Implanter Designed to Address Unique High Dose Implant Applications Atul Gupta, Michael Ameen, Andy Ray and Richard Rzeszut; Axcelis Technologies, United States

SESSION TU3: Annealing Technologies and Processes I
Tuesday Afternoon, September 27, 2022
Presidential Ballroom, Second Level, Salons C&D

2:00 PM *TU3.01
Flash Lamp Annealing of Semiconductor Materials L. Rebohle[1,2]; [1]Helmholtz innovation blitzlab, Germany; [2]Helmholtz-Zentrum, Germany

2:30 PM TU3.02
Influence of N Doping on the Crystallization Kinetics of Phase Change Materials ($Ge_2Sb_2Te_5$) Minh Anh Luong[1], Nikolay Cherkashin[1], Béatrice Pecassou[1], Chiara Sabbione[2], Frederic Mazen[2] and Alain Claverie[1]; [1]CEMES-CNRS, France; [2]Léti/CEA, France

2:50 PM TU3.03
Time Resolved Reflectometry with Pulsed Laser Melting of Implant Amorphized $Si_{1-x}Ge_x$ Thin Films Jesse A. Johnson[1], Xuebin Li[2], Christopher Hatem[3], David Brown[1], Bruce Adams[2] and Kevin S. Jones[1]; [1]University of Florida, United States; [2]Applied Materials, Inc., United States; [3]Applied Materials – Varian Semiconductor Equipment, United States

3:10 PM TU3.04
Optimization of Solid Phase Epitaxial Regrowth Assisted by UV Nanosecond Pulsed Laser Angela Alvarez Alonso[1], Pablo Acosta Alba[1], Eloïse Rahier[2,3], Sébastien Kerdiles[1], Nicolas Gauthier[1], Nicolas Bernier[1] and Alain Claverie[2,3]; [1]CEA-LETI, France; [2]Centre d'Élaboration des Matériaux et d'Etudes Structurales, France; [3]Centre National de la Recherche Scientifique, France

3:30 PM TU3.05
Continuum Simulations of the Evolution of Faulted and Perfect Dislocation Loops in Silicon During Post-Implantation Annealing Anna Johnsson; Fraunhofer Institute for Integrated Systems and Device Technology IISB, Germany

SESSION TU4: Plenary Session II
Tuesday Afternoon, September 27, 2022
Presidential Ballroom, Second Level, Salons C&D

3:50 PM **TU4.01
Integration Technologies for *pn*-Stacked TMDC CMOS Devices Hitoshi Wakabayashi; Tokyo Institute of Technology, Japan

SESSION PS1: Poster Session I: Implant/Doping Technologies and Processes
Tuesday Afternoon, September 27, 2022
4:30 PM - 5:30 PM
Presidential Ballroom, Second Level, Salons A&B and Foyer

PS1.01
The Performance of the Fourth Generation of Safe Delivery Source® (SDS®4) Package on AIBT iPulsar High Current Implanter Ying Tang[1], Vito Nien[1], Weihang Guan[1], Eric Tien[1], Luke Hu[2], Te-Min Wang[2], Cheng-Mao Chien[2] and Brandon Ni[2]; [1]Entegris, Inc., United States; [2]AIBT Inc., Taiwan

PS1.02
Investigation of Various Source Materials and Co-Gases for Fluorine Ion Implantation Performance Improvement Ying Tang, Joseph Despres, Joseph Yoon, Matt Marlow and Joseph Sweeney; Entegris, Inc., United States

PS1.03
Germanium Ion Implantation Performance Improvement on Applied Materials' VIISta HCS High Current Implanter with Use of Germanium Tetrafluoride (GeF_4) and Hydrogen (H_2) Mixture Gases Ying Tang[1], Chee Weng Leong[1], Han Keong Lim[2], Chee King Tiu[2], Eric Tien[1], Joseph Despres[1] and Joseph Sweeney[1]; [1]Entegris, Inc., United States; [2]GlobalFoundries Semiconductor Manufacturing Company, Singapore

PS1.04
Performance Improvement on SMIT SHX-III High Current Ion Implanter through the use of EnrichedPlus ^{72}Germanium Tetrafluoride (enPLUS $^{72}GeF_4$) and Hydrogen (H_2) Mixture Gases Ying Tang[1], Vito Nien[1], Page Ku[2], Henry Yang[2], Tommy Lin[2], Will Chen[2], Eric Tien[1], Joseph Despres[1] and Joseph Sweeney[1]; [1]Entegris, Inc., United States; [2]Micron Technology, Inc., Taiwan

PS1.05
Investigation of Source Materials, Co-gases, and Methods for Aluminum Ion Implantation Ying Tang, Ed Jones, Joseph Despres, Kavita Murthi and Joseph Sweeney; Entegris, Inc., United States

PS1.06
Performance and Reliability of the Fourth Generation of Safe Delivery Source® (SDS®4) in the Ion Implantation Application Weihang Guan, Ying Tang, Timothy Dwyer, Ed Jones, Joseph Despres and Kavita Murthi; Entegris, United States

PS1.07
Charge Transport in Doped and Strongly Coupled Nanocrystal Films Ji-Hyuk Choi; Korea Institute of Geoscience and Mineral Resources, Korea (the Republic of)

PS1.08
Results and Adoption of Safe Delivery Source® (SDS®4) on VIISta® HCP Barry Chambers[1] and Douglas Newman[2]; [1]Entegris, Inc., United States; [2]Texas Instruments Inc., United States

PS1.09
How Safe Is a Safe Dopant Gas Delivery System? Jose Arno, Mitch Weston and Patrick Fuller; NuMat Technologies, United States

PS1.10
Dopant Gas Purity and Adsorbent Stability Jose Arno, Omar Farha, William Morris, John Siegfried, Glenn Tom, Mitch Weston and Patrick Fuller; NuMat Technologies, United States

PS1.11
Temperature Effect in High Dose, Medium Energy Implantation with Single-Wafer-Type Implanter Takuya Sakaguchi, Kazutaka Tsukahara, Tae Hoon Huh and Yoji Kawasaki; Sumitomo Heavy Industries Ion Technology Co., Ltd., Japan

PS1.12
Ionization Induced Carbon Phase Changes in Graphite Daryush Ila; University of West Georgia, United States

PS1.13
Enhancement of Al^+ Beam Current in GSD III-180 Hiroki Murooka; Sumitomo Heavy Industries Ion Technology Co., Ltd., Japan

PS1.14
A Study of Beam Divergence Effects for Medium Dose Channeling Implants Tae Hoon Huh, Akira Mineji, Noriyuki Suetsugu and Yoji Kawasaki; Sumitomo Heavy Industries Ion Technology, Japan

PS1.15
Ion Erosion and Particle Release in Fine Graphite Michael Current[1], Hideto Fujibuchi[2], Takahiko Ido[3], John Schuur[4] and Max Slaton[5]; [1]Current Scientific, United States; [2]Ibiden, United States; [3]Ibiden Japan, Japan; [4]II_VI Implant Foundry, United States; [5]Covalent Metrology, United States

PS1.16
Profiles and Defects in Highly-channeled and Random Beam Orientation MeV Dopant Implants in Si(100) Michael Current[1], Yoji Kawasaki[2], Takuya Sakaguchi[2], Anita Pongracz[3] and Viktor Samu[3]; [1]Current Scientific, United States; [2]Sumitomo Heavy Industries Ion Technology, Japan; [3]Semilab, Hungary

PS1.17
PL and SRP Studies of Phos Implants Michael Current[1], Yoji Kawasaki[2], Taehoon Huh[2], Viktor Samu[3] and Luca Sinko[3]; [1]Current Scientific, United States; [2]SMIT, Japan; [3]Semilab, Hungary

PS1.18
Ion Erosion and Elemental Purity of Deposited Films on Al Walter Wriggins[1], John Schuur[2], Matthew Wong[3], Avery Green[3] and Michael Current[4]; [1]II_VI Disk Refurbishment, United States; [2]II-VI Implant Foundry, United States; [3]Covalent Metrology, United States; [4]Current Scientific, United States

PS1.19
Individual Dopant Profiles in High Energy Multiple Implantation Under Channeling Conditions Yoji Kawasaki, Haruka Sasaki, Makoto Sano and Mitsuaki Kabasawa; Sumitomo Heavy Industries Ion Technology, Japan

PS1.20
Beam Shape Control System by Machine-Learning on the NISSIN BeyEX Medium Current Ion Implanter Shinya Takemura, Shigeki Sakai and Eiichi Murayama; Nissin Ion Equipment Co.,Ltd., Japan

PS1.21
Scaled FinFET Well Formation Using Heated Implantation Baonian Guo, Nilay Pradhan, Yan Zhang, Hans J. Gossmann, Hans V. Meer, Benjamin Colombeau and Kyuha Shim; Applied Materials, Inc., United States

PS1.22
Analysis of Dopant Distribution Profiles of Very High Energy Implants Serguei Kondratenko and Leonard Rubin; Axcelis Technologies, Inc., United States

PS1.23
Neutron Radiation due to High Energy Boron Ion Beams Wilhelm P. Platow, Leonard Rubin, Patrick Mayfield, R. Lessard, Paul Whalen and Steve Roberge; Axcelis Technologies, United States

PS1.24
Assessment of a 2MeV Li+ Ion Beam Resolution by means of the Ion Beam Induced Charge Technique. Greta Andrini[1,2], Elena Nieto Hernández[3,2], Georgios Provatas[4], Marko Brajković[4], Andreo Crnjac[4], Sviatoslav Ditalia Tchernij[3,2], Jacopo Forneris[3,2], Valentino Rigato[2], Matteo Campostrini[2], Zdravko Siketić[4], Milko Jakšić[4] and Ettore Vittone[3,2]; [1]Politecnico di Torino, Italy; [2]Istituto Nazionale di Fisica Nucleare (INFN), Italy; [3]University of Turin, Italy; [4]Ruder Boskovic Institute, Croatia

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SESSION WE1: Advanced Metrologies for Implant/ Doping and Annealing Processes I
Wednesday Morning, September 28, 2022
Presidential Ballroom, Second Level, Salons C&D

9:00 AM *WE1.01
Metrologies to Study Ion Implanted Semiconductor Materials Temel Buyuklimanli; Eurofins, United States

9:30 AM WE1.02
Lateral Mapping of Damage Patterns in Plasma Immersion Ion Implanted Silicon Orsolya Kéri[1], Árpád Kerekes[1], János Szivós[1], Attila Sütö[1], Badeeb Leila[1], Dániel Péter Szekrényes[1], Ferenc Korsós[1], György Nadudvari[1], John Byrnes[2] and Zsolt Zolnai[1]; [1]Semilab Hungary Ltd, Hungary; [2]Semilab USA, United States

9:50 AM WE1.04
Measuring Sub-nm Activation Profiles in Very Highly Doped Semiconductors Abhijeet Joshi and Bulent M. Basol; Active Layer Parametrics, Inc., United States

10:10 AM BREAK

SESSION WE2: Advanced Technologies and Processes
Wednesday Morning, September 28, 2022
Presidential Ballroom, Second Level, Salons C&D

10:40 AM *WE2.01
NS-Pulsed Melt Laser Annealing for Advanced CMOS Contacts Toshiyuki Tabata[1], Karim Huet[1], Fulvio Mazzamutro[1], Jean-Luc Everaert[2], Edward Moore[3], Leonard Rubin[3] and Dwight Roh[3]; [1]Laser Systems & Solutions of Europe (LASSE), France; [2]imec, Belgium; [3]Axcelis Technologies, Inc., United States

11:10 AM WE2.02
The Detail Analysis of Behavior of Heavy Metals In 4H-SiC Ryota Wada, Tsutomu Nagayama, Takashi Kuroi and Nariaki Hamamoto; Nissin Ion Equipment CO., LTD., Japan

11:30 AM WE2.03
Comparative Evaluation of Indirectly Heated Cathode DC Ion Source and Inductively Coupled Plasma RF Ion Source at High Current Ion Implanter. Jongjin Hwang[1,2]; [1]SK hynix, Korea (the Republic of); [2]Hanyang University, Korea (the Republic of)

11:50 PM WE2.04
Risk of Neutron Generation with Implantation of Light Ions Jeremy A. Turcaud, Christopher Heckman, Valarie Heckman, Ahmet Hassan, Raymond Pong and John Schuur; II-VI Incorporated, United States

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SESSION TH1: Annealing Technologies and Processes II
Thursday Morning, September 29, 2022
Presidential Ballroom, Second Level, Salons C&D

9:00 AM *TH1.01
Millisecond and Sub-Millisecond Annealing Jacob M. Jensen; Intel, United States

9:30 AM TH1.02
Ion Implantation and Activation of Aluminum in Bulk 3C-SiC and 3C-SiC on Si Frank Torregrosa[1], Roberta Nipoti[2], Fan Li[3], Marica Canino[2], Fabrizio Tamarri[2], Gael Borvon[1], Benjamin Roux[1], Stephane Morata[1] and Marcin Zielinski[4]; [1]IBS (Ion Beam Services), France; [2]Consiglio Nazionale delle Ricerche, Italy; [3]University of Warwick, United Kingdom; [4]NOVASiC, France

9:50 AM TH1.03
Fabrication of Nano- to Micro-Scale Optical Structures in Silica Daryush Ila; University of West Georgia, United States

SESSION PS2: Poster Session II: Advanced Implant/Doping and Annealing Equipment
Thursday Morning, September 29, 2022
10:10 AM - 11:30 AM
Presidential Ballroom, Second Level, Salons A&B and Foyer

PS2.01
IMPHEAT-II, A Novel High Temperature Ion Implanter for SiC Power Devices Yusuke Kuwata; NISSIN ION EQUIPMENT, Japan

PS2.02
Electrostatic Ion Implant Chuck with Fast Declamp Response Through Charge Control Jakub Rybczynski, Steven Donnell, Isaac Parker, Caleb Minsky and Chandra Venkatraman; Entegris, Inc., United States

PS2.03
New Control System of the Multiple Filaments in the Large Ion Source for Ion Doping System iG6 Ver.2 Yuya Hirai[1], Kenji Watari[1], Koichi Orihira[1], Takeshi Matsumoto[2], Junichi Tatemichi[1] and Yutaka Inouchi[1]; [1]Nissin Ion Equipment Co., Ltd, Japan; [2]Nissin Ion Equipment USA Inc., United States

PS2.04
A Newly Developed ECR Ion Source with Wide Dynamic Range of Beam Current Suguru Itoi, Hideki Fujita and Shigeki Sakai; Nissin Ion Equipment, Japan

PS2.05
Linac Simulation with Dataset Generator Wilhelm P. Platow, Shu Satoh and Neil J. Bassom; Axcelis Technologies, United States

PS2.06
Improvements Enabled in SiC Power Devices by Advancements in Ion Implantation Hardware Pratim Palit, Stephen Krause, Shardul Patel and William Bogiages; Varian Semiconductor Equipment, United States

PS2.07
Ion Implanter Beam Optics Design Using Global Optimization Techniques Bo Vanderberg, Steve Drummond and Joe Valinski; Axcelis Technologies, Inc., United States

PS2.08
Purion XEmax, Axcelis Ultra High Energy Implanter with Boost Technology Shu Satoh, Wilhelm P. Platow, Serguei Kondratenko, Leonard Rubin, Patrick Mayfield, Genise Bonacorsi, Paul Whalen and Russell Newman; Axcelis Technologies, United States

PS2.09
Unique Features of FLEXion Tool for Wide Band Gap and III-V Semiconductor Devices Fabrication Gilles Mathieu, Stephane Morata, Gilles Boccheciampe, Benjamin Roux and Frank Torregrosa; IBS (Ion Beam Services), France

SESSION PS2: Poster Session II: Advanced Metrologies for Implant/Doping and Annealing Processes Thursday Morning, September 29, 2022
10:10 AM - 11:30 AM
Presidential Ballroom, Second Level, Salons A&B and Foyer

PS2.10
Compositional Measurement of Confined SiGe Devices with Self Focusing SIMS Anne-Sophie Robbes[1], Paula Peres[1], Kilian Soulard[1], SeoYoun Choi[1], Rong Liu[1], Olivier Dulac[1] and Dan Jacobson[2]; [1]CAMECA, France; [2]CAMECA Instruments, Inc., United States

PS2.11
Detection of Particles in the Ion Beam Aki Ninomiya[1], Hiroshi Matsushita[1], Sayumi Hirose[2], Takanori Yagita[1], Takao Morita[1] and Hiroyuki Kariya[1]; [1]Sumitomo Heavy Industries; Ion Technology Co., Ltd., Japan; [2]Sumitomo Heavy Industries, Ltd./, Japan

PS2.12
Reduction of Wafer Charging Effects with Advanced Electrostatic Chuck Technologies Robert T. Fryer, Christina Sohl, Wade Krull and Kevin Wenzel; Axcelis Technologies, Inc., United States

PS2.13
Sheet-Resistance Measurement for Ultra-High Energy Ion Implantation Haruka Sasaki, Takuya Sakaguchi and Yoji Kawasaki; Sumitomo Heavy Industries Ion Technology, Japan

PS2.14
Low Temperature Monitoring with Implantation and Silicidation Ende Lutz[1], Martin Grund[1], Juergen Niess[2] and Wilfried Lerch[3,4]; [1]XFAB, Germany; [2]HQ-Dielectrics GmbH, Germany; [3]Fraunhofer Research Institution for Microsystems and Solid State Technologies EMFT, Germany; [4]Skylark Solutions, Germany

PS2.15
Physical, Electrical and Electrochemical Characterization of 2D Materials (Graphite, GNP and GO) Sonjoy Dey and Gurpreet Singh; Kansas State University, United States

SESSION PS2: Poster Session II: Modeling and Simulation of Implant/Doping and Annealing Processes
Thursday Morning, September 29, 2022
10:10 AM - 11:30 AM
Presidential Ballroom, Second Level, Salons A&B and Foyer

PS2.16
Ion Implantation Simulation and Optimization in Semiconductor Compounds Jeremy A. Turcaud, John Schuur and Raymond Pong; II-VI Incorporated, United States

SESSION PS2: Poster Session II: Device Applications for Implant/Doping and Annealing Processes
Thursday Morning, September 29, 2022
10:10 AM - 11:30 AM
Presidential Ballroom, Second Level, Salons A&B and Foyer

PS2.17
Optimization of Doped Lanthanated Tungsten Components in Ion Sources by Determining the Temperature Profile for Halogen Processes Florian H. Schaper[1], Karl-Heinz Leitz[1], Harald Köstenbauer[1] and Stefan Schulz[2]; [1]PLANSEE, United States; [2]Infineon Technologies Dresden GmbH & Co. KG, Germany

PS2.18
Cryogenic Implantation to Boost PFET Performance and Improve Variability in 3D NAND Flows Jeng_Hwa Liao[1], Jung-Yu Hsieh[1], Ling-Wu Yang[1], Tahone Yang[1], Kuang-Chao Chen[1], Baonian Guo[2], Monica Hsiao[2], Shiryu Lee[2], fenglin Wang[2], Sungho Jo[2] and Kyuha Shim[2]; [1]Macronix, Taiwan; [2]Applied Materials, Inc., United States

PS2.19
Angle-Directed Ion Beams for Localized Deposition on High Aspect Ratio Structures Michael Current[1], Thomas E. Seidel[2]; [1]Current Scientific, San Jose, CA, United States; [2]Seitek50, Pam Coast, FL, United States

SESSION TH2: Advanced Metrologies for Implant/Doping and Annealing Processes II
Thursday Morning, September 29, 2022
Presidential Ballroom, Second Level, Salons C&D

11:30 AM *TH2.01
Review of Applications of Defect Photoluminescence Imaging (DPLI) to Monitoring Crystallographic Defects During IC Processing Lubek Jastrzebski; Semilab, United States

12:00 PM TH2.02
Advanced Process Control Method for Inline Isolation Implant Monitoring in III-V GaAs Semiconductor Fabrication Sasha Kurkcuoglu and Shiban Tiku; Skyworks Solutions, Inc., United States

12:20 PM TH2.03
Defect Microstructure in Ion Implanted GaN Andrzej W. Turos; Institute of Microelectronics and Photronics, Poland

SESSION TH3: Implant/Doping Technologies and Processes
Thursday Afternoon, September 29, 2022
Presidential Ballroom, Second Level, Salons C&D

2:00 PM *TH3.01
More Than Moore Applications of Nanosecond Laser Annealing Sébastien Kerdiles[1]; [1]Commissariat à l'Energie Atomique et Aux Energies Alternatives, France

2:30 PM TH3.02
Silicon Damage from Timescale Modulation for Dose Accumulation in Single Implant and Damage Interactions Between Multiple Implants James S. DeLuca and Gary Cai; Axcelis Technologies, United States

2:50 PM TH3.03
Defects and Dopants Behavior of Medium Dose Range Implant into Heated Silicon Wafers Tae Hoon Huh, Akira Mineji and Yoji Kawasaki; Sumitomo Heavy Industries Ion Technology, Japan

3:10 PM BREAK

SESSION TH4: Advanced Materials
Processing & Closing Remarks
Thursday Afternoon, September 29, 2022
Presidential Ballroom, Second Level, Salons C&D

3:40 PM *TH4.01
Metal/Semiconductor Contact Investigations for Applications in Advanced CMOS Technology Hao Yu, Marc Schaekers, Jean-Luc Everaert, Naoto Horiguchi, Nadine Collaert and Kristin De Meyer; imec, Belgium

4:10 PM TH4.02
Strain Characterization of Si+Ge, SiGe+Ge, SiGe+C, Ge+C, Ge+Sn & Si+Ge+Sn Thin Layers Formed By Implantation With RTA or Laser Melt Annealing Using SIMS, XPS, EDX-TEM, Raman and XRD Analysis John O. Borland; J.O.B. Technologies, United States

4:30 PM TH4.03
Nitride Stress Inversion Using Plasma Immersion Ion Implantation Laurent Lachal[1], Christophe Plantier[1], Frank Torregrosa[2], Cedric Aubert[2], Jean-Michel Pedini[1], Gael Borvon[2], Marianne Coig[1], Frederic Milesi[1], Heimanu Niebojewski[1] and Frederic Mazen[1]; [1]Univ. Grenoble Alpes, CEA-LETI, France; [2]Ion Beam Services, France

4:50 PM TH4.04
Key Physical Features and Applications of High Energy Ion Implantation Using the Energy-Filter Technology Michael E. Rueb[1,2], Shavkat Akhmadaliev[3], Constantin Csato[2], Stefan Illhardt[2], Hitesh Jayaprakash[1,2] and Florian Krippendorf[2]; [1]University of Applied Sciences Jena, Germany; [2]mi2-factory GmbH, Germany; [3]Helmholtz-Zentrum Dresden-Rossendorf, Germany

5:10 PM
Closing Remarks - - Presented by Susan Felch, IIT 2022 Co-Chair

Development of Ultra-High-Current Implanter for Material Modification Process in Next Era Devices

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Many efforts have been devoted to realize continuous scaling of device size and to improve device performance. This results in complex device structures and many process steps. Material modification using ion doping is one of the promising candidates to overcome these issues [1]. We have newly developed ion implant system for this application. This new tool features extremely high current beams with low energy and it enables the material modification process as a manufacturing worthy step from the viewpoint of productivity. It has 30WPH～42WPH throughput for high doses with 1.0×10^{16} ions / cm^2 even at low energies of less than 1 keV.

Sheet beams extracted with a height of about 300 mm from the ion source are separated by the mass analyzing magnet and pass through electrostatic energy filters to eliminate energy contamination before arriving at a wafer. This tool achieves high beam transport efficiency from the ion source to the wafer by optimizing the beam optical system such as shortening the beamline. The beams at the wafer are long and uniform along the vertical direction and the process is carried out by horizontal wafer scanning.

As an example of material modification using ion implant, Fig 1 shows dose-dependency of Dry etching rate for SiO_2 film by P^+ doping at 2keV. The CF_4 gas was utilized as an etchant for ECR plasma etching. It is found that the etching rate after the dose of 1.0×10^{16} ions / cm^2 doping was more than 1.5 times as large as that without doping. This remarkable high beam current tool would be expected to realize many novel applications.

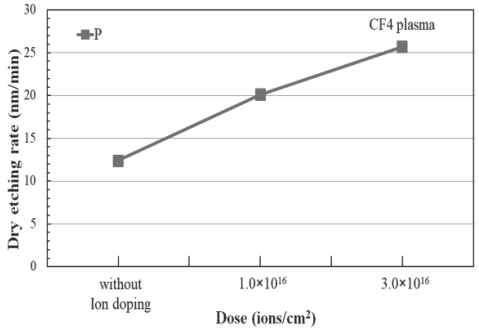

Fig1 Dose dependency of dry etching rate for SiO2.

[1] R Wada et al., Jpn. J. of Applied Physics 59 SGGA03 (2020)

Particle counts and size distributions after implantation with on-wafer graphite sources

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Many studies of particle effects arising from choices for graphite materials and surface treatments and locations of beam line components require extensive efforts to rebuild and reconfigure operating implant tools followed by particle count measurements on implanted wafers which are consequently "indirect". This study reports an effort to strongly reduce the distances from graphite "source" surfaces and the particle measurement area by mounting various types of graphite directly onto Si wafers. This approach also allows for the implants to be carried out in an unmodified implantation system.

In this experiment, thin pieces of graphite were mounted into etched recesses in the outer regions of 200 mm Si wafers, leaving a bare 100mmD central area for particle measurements. 8 different graphite samples, with various surface treatments, were mounted on separate wafers, with 4 graphite pieces per wafer. Each wafer was implanted in a serial wafer processing implanter with sequential cycles of 40 keV BF_2^+ implants at individual doses of 5e15 B/cm^2, with Surfscan particle scans prior to and after each implant cycle. Post-implant graphite surface textures and grain size distributions were imaged by SEM and electron backscattering methods.

Systematic differences were observed in the total particle counts and particle size distributions for the various graphite samples. Trends are compared to graphite bulk and surface properties.

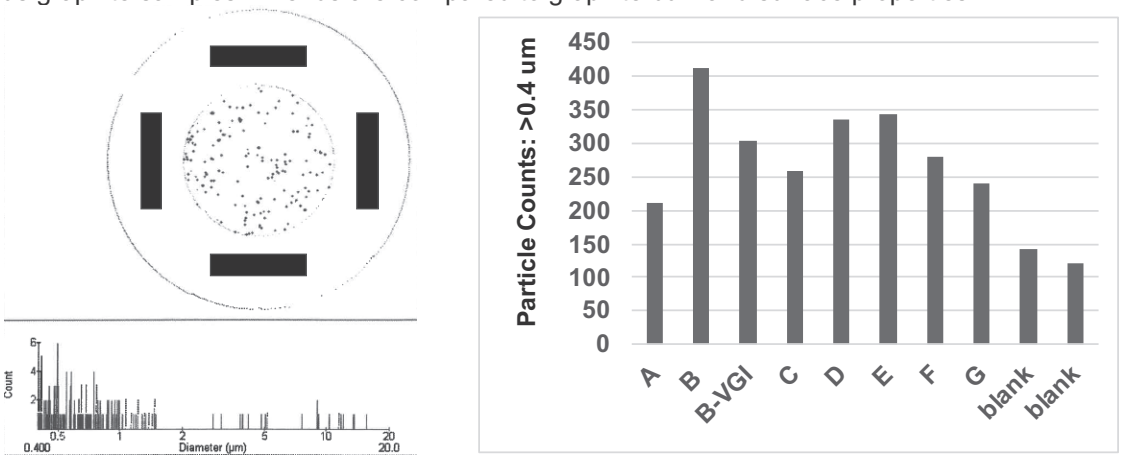

Figure 1. Example Surfscan particle map and size distribution, showing the location of 4 thin graphite pieces mounted into etched recesses in the outer wafer regions and a central 100 mmD particle scan area of a 200 mm wafer (left) and the sum of particle counts for 8 graphite types and 2 blank Si wafers (right). .

High Temperature Electrostatic Chuck Enabled by BN Dielectrics

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High temperature ion implantation followed by annealing is a common practice in SiC device fabrication. An electrostatic chuck (ESC) is the preferred wafer handling apparatus in ion implantation. The typical ESC structure contains a dielectric base, a set of electrodes, and a thin dielectric cover layer. To establish a proper Johnsen-Rahbek (J-R) chuck force, the resistivity of the dielectric layer between the wafer and electrode needs to be controlled in the range of 10^9 ~ 10^{13} Ω-cm. The electrical resistivity of conventional ceramics, Al_2O_3 and AlN, decreases rapidly with rising temperature, which introduces challenge to ion implantation with temperature greater than 400°C. In this study, we present the properties of pyrolytic boron nitride (PBN) and the performance of ESCs based on this dielectric material.

A ceramic layer of PBN with hexagonal lattice structure was prepared by chemical vapor deposition with BCl_3 and NH_3 at a temperature >1500°C. Hydrocarbon species were sometimes added to induce carbon into the PBN lattice (C-PBN) for resistivity tuning. The resistivities of PBN and C-PBN were measured at various temperatures and compared to AlN (Fig. 1). While AlN's sharp resistivity transition results in a narrow low-temperature J-R chuck operation, PBN presents a resistivity order of magnitude higher which enables J-R function up to 1050°C. Adding carbon into PBN (C-PBN) achieves a much flatter resistivity slope that is suitable for wide chuck operation from sub-zero to 800°C. Subsequently, an electrostatic chuck, as illustrated in Fig. 1, was constructed through multilayer CVD coating and patterning technologies. Thanks to PBN's high resistivity and dielectric strength, electrical breakdown is effectively prevented under intense heat. Typical chucking force of 10^4 Pa could be established with a voltage of +/-1 kV. In addition, all the construction materials, graphite, PBN and pyrolytic graphite (PG), have high thermal shock resistance and low thermal mass. As the result, the PBN based ESC can reach the target temperature with exceptionally fast speed without cracking or delamination (Fig. 2). With the intimate wafer-chuck contact, a consistent wafer thermal profile with good uniformity of 1.1% was achieved at temperature of 600 ~ 800°C on a 200 mm wafer using single zone heating.

In summary, dielectrics, PBN and CPBN, with their unique high temperature resistivity profiles enabled the J-R chucking operation beyond the conventional ceramic ESC capability. Combining with PG and graphite, the dual-functioned PBN ESC achieved high chuck force and good thermal uniformity with fast response at elevated temperature. This ESC technology provided a viable solution to the wafer heating and handling challenges in the SiC ion implantation application.

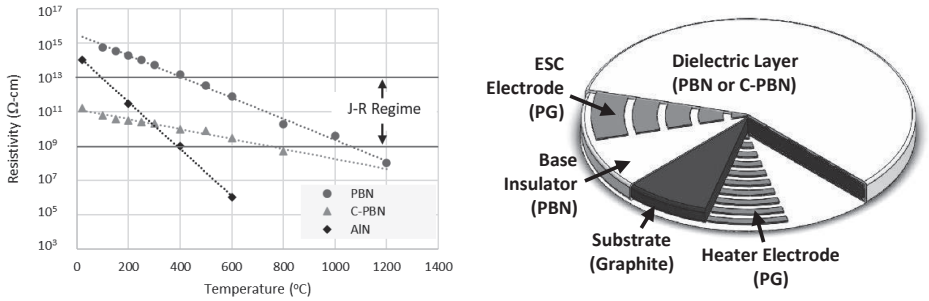

Fig. 1. Left: Resistivity comparison between PBN, C-PBN and AlN at elevated temperature; Right: Illustration of an integrated ESC and heater

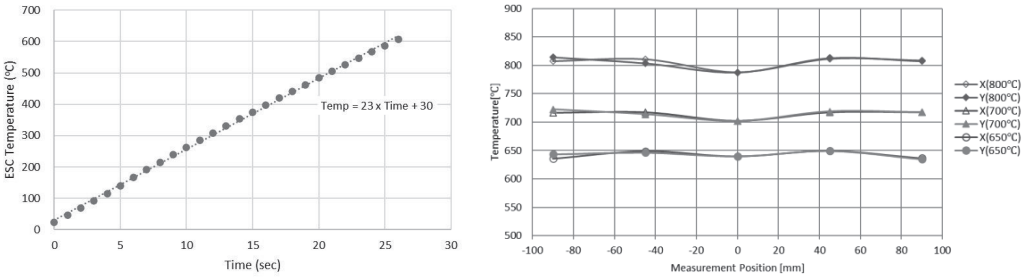

Fig. 2. Left: PBN ESC temperature ramping at the rate of 23°C/sec; Right: Temperature profile of a 200 mm wafer on a PBN ESC

Technical Developments of Thermal Annealing in the Past Sixty Years, and Future Perspectives [i]

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Since ~ 60 years the IC is such a success that its supply chain is now even facing shortages. Driving force behind this success is the continuing scaling of feature sizes in logic and memory ICs, with lower cost per transistor and power consumption. Scaling was possible by continuous advancement in thin-film deposition, photolithography, reactive ion etching and, last but not least, ion implantation annealing.

In the 1960's, single-wafer RTA with its low thermal mass and tight ambient control as compared to multi-wafer furnace annealing, showed its potential as core technology in ULSI device manufacture: IBM pioneered on sub-µm Si diodes by using pulsed laser beams on B-doped Si with paint-on P. In the 1970s RTA was dominated by pulsed laser annealing. Other short-time heating methods followed, like graphite strip heaters, pulsed e-beams and Bell Labs' ground breaking work with flash lamps. In the 1980s flood heating with W-halogen and arc discharge lamps took pulse annealing into the 1-100 sec process regime. Thus, lamp-based ion implant annealing enabled source/drain dopant activation w/o dopant redistribution.

Until the mid-1990s the only obstacles for full industrial acceptance of single-wafer RTA, also called Rapid Thermal Processing (RTP), were **1**) reproducible temperature measurement, irrespective of multilayer stacks or patterns present on the wafer, reactive ambient gas or layers formed at the wafer backside, and **2**) temperature uniformity across the wafer during the entire process. By ~2000 when 1Gb DRAM was nearing full production these obstacles were overcome: the so-called ripple pyrometer offered independent, reproducible temperature control, and temperature uniformity by using dynamic and individual power control of ring-shaped lamp zones. Also, the wafer's effective emissivity (thus absorptivity) was increased by using reactor chambers with highly reflective cavity or black-cavity "kaleidoscope" type designs.

RTP is now a routine process with ramp rates of >100 ^{o}C/s and high-temperature soak times of ~1 sec in many semiconductor applications: source/drain implant annealing, contact alloying, self-aligned ("salicide") $TiSi_2$ and $CoSi_2$ interconnects, formation of refractory nitrides, silicides, and thin gate dielectrics formation; glass reflow, deposition in reactive gases like CVD of amorphous and poly-Si, epitaxial Si and Ge_xSi_{1-x}, and tungsten, etc. Other application fields are in back-end processing, like packaging or solder reflow, and in the processing of III-V and other compound semiconductors.

Today's ultra-shallow *p-n* junction formation in modern CMOS requires state-of-the-art implant annealing to meet today's criteria in junction depth, profile abruptness, and sheet resistance. Often this can only be fulfilled by reducing the temperature budget (i.e. *temperature* x *time*). One approach is using flash-assisted RTP where the wafer is first conventionally heated to an intermediate background temperature and then an ultrashort (milliseconds) high-energy flash-lamp 'spike' heats the wafer. Only this way the single-digit nm diffusion lengths of dopants, and other side reactions will be sufficiently suppressed to allow future technology nodes. The other extreme in "hotter and faster" processing is in lower-temperature plasma-assisted processing,

Next to the technical history this keynote will discuss ● Fundamental thermophysics in RTP: ● General RTP system components ● Temperature non-uniformity

Finally, some on the present and future perspectives: in non-planar (3D) device architectures such as FinFETs new issues arise. Conventional ion implantation is still the mainstay technology, but new techniques in deposition and plasma doping are emerging. Examples as in Monolayer Doping and subsequent annealing of 3D silicon devices have better potential to achieve conformal doping. Also, the introduction of Ge- or III-V based channel materials will influence the behavior of dopants and defects. Ge is easier amorphized than Si and the damage generation mechanism in Ge is not sufficiently understood. This holds even more so for high-mobility III-V channels. Likewise, Ge oxidation is still under investigation, e.g., in processes using RTP-assisted low-temperature microwave plasmas.

This keynote will end with possible other applications emerging in semiconductor processing such as RTA-assisted Atomic Layer Deposition & Etching. Also emerging fields in processing "*beyond semicon*" are ceramic and magnetic films, as well as in flat panel display processing and in photovoltaics.

[1] A 5-page extended abstract can be requested from the author: f.roozeboom@utwente.nl

35 Years of Challenge and Innovation in Ion implant

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Over the last 35 years the implant industry has faced a number of technical challenges. Usually, but not always, these are brought on by semiconductor scaling causing a change of dimensions, materials, or topologies. So far, each time that has caused a problem for the existing technology, there has been an innovation that has saved the day. Some innovations, like the plasma flood gun now seem relatively minor. Others, like single wafer implantation changed the industry. We will review several of these critical innovations.

Smart Cut, FD-SOI and integration challenges

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Emerging electronic applications such as Internet-Of-Things (IOT), mixed signal processing or silicon photonics require silicon-on-insulator substrates (SOI) with very challenging specifications. For example, as threshold voltage of FD-SOI transistor depends directly on the thickness of the top silicon layer, the thickness and the surface roughness have to be controlled within extremely tight tolerance. The Smart-Cut™ process is the only technology compatible with high volume manufacturing that allows transferring extremely thin layers of crystalline material with respect to these requirements. Furthermore, the layer transfer can be achieved on a wide range of functionalized handling substrates that can bring an additional gain to the final device.

This presentation aims to describe the key challenges in the manufacturing this new generation of SOI wafers. An overview of FD-SOI substrates and their applications will be done, highlighting the specificity in terms of structure requirements. The critical steps in SOI fabrication will be described, with emphasis on the need to physically model the manufacturing processes and to develop new specific metrology. Examples of new use of RTP processes to overcome the current limitations will be given.

Experiments and Modelling to Understand Implanted Layer Exchange Production of Isotopically Pure Si and Ge Layers for Quantum Computers

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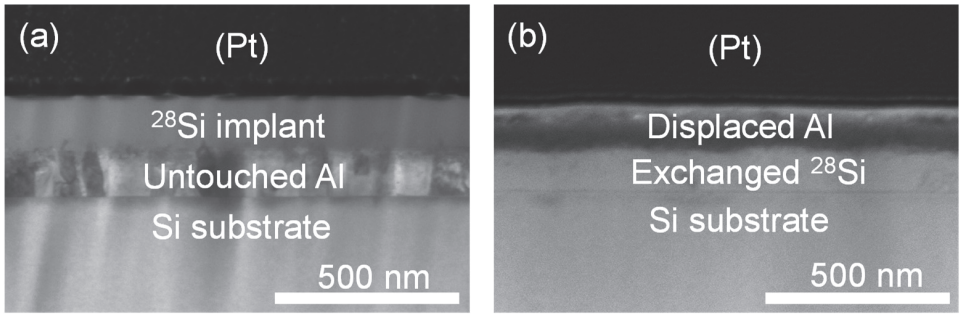
Donor spin qubits hosted in silicon are attractive quantum computing architectures with long coherence times, scalability and compatibility with CMOS industrial manufacturing. An isotopically pure ^{28}Si layer is spin-free and therefore, when cryogenically cooled, can act as a "solid-state vacuum" - an ideal environment to isolate quantum qubit states for computational operations. Having a readily available source of ^{28}Si is essential to research and future mass production of quantum computers. We are developing an implanted layer exchange (ILE) process [1,2] to produce isotopically pure Si and Ge layers for the manufacture of quantum computers. ILE uses standard implantation to implant ions of a single isotope into the surface of an Al film deposited on a substrate wafer. A post implant, layer exchange anneal causes the isotopically selected atoms to diffuse through the Al and grow on the substrate.



False colour BF STEM images of the ^{28}Si ILE enrichment process: (a) ^{28}Si/30keV/6.7x10^{16} cm^{-2} ion implantation into Al on Si; (b) after 500°C / 1 min layer exchange anneal.

ILE allows implantation energies to be used where beam transmission is maximised, requires lower fluences compared to enrichment by direct implantation into Si, overcomes surface oxidation (negating the need for a UHV endstation) and self-getters isobaric impurities. A major challenge is to achieve an acceptable residual Al concentration in the ^{28}Si layer. The ultimate ILE process would produce non-defective, single crystal, isotopically pure, ^{28}Si or ^{74}Ge layers of uniform thickness containing no Al contamination. We believe a key route to achieving these goals is to ensure that ions implanted into the surface of an Al film rapidly diffuse during the anneal to epitaxially grow on a substrate rather than nucleate at grain boundaries in the Al. To develop this idea, we have compared ILE of Si after large area implants in a Danfysik beamline implanter to ILE of Ge after small area (100 micron²) implants using a SIMPLE (FIB based) implanter [2]. Suppressing epitaxial growth during the anneal by damaging the substrate surface via implantation or by poor removal of native oxide before Al deposition did indeed lead to the formation of large poly crystals, observed using top down optical and secondary electron microscopy and cross sectional TEM. Interpretation of these observations has been aided by the use of TRIDYN [3] to model the implant profiles. A kinetic Monte Carlo model based on SPPARKS [4] is being developed to investigate the mechanisms that compete during the anneal part of the layer exchange process. We will present a selection of our observations and current understanding that identify the greatest challenges that will need to be overcome if we are to perfect our ILE method.

[1] Schneider, England, J Phys D submitted 2022
[2] England et al NIMB 461 (2019) 30
[3] Moller, Eckstein NIMB 2 (1984) 814
[4] Plimpton et al https://spparks.github.io

TEM Investigation of Extended Defects in Aluminum Implanted 4H-SiC Substrates

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Silicon carbide (SiC) is a promising wide bandgap material with excellent electronic properties suitable for next-generation power devices. However, the necessary combination of ion implantation with high temperature annealing (>1700^{o}C) to introduce and activate dopants induces large amounts of irreversible lattice damage. Specifically, the formation of extended defects, such as basal plane dislocations and stacking faults, has been extensively reported in samples that contain a homoepitaxially grown layer on SiC wafers after the annealing process. Though an epilayer is typically used for device fabrication, quality of bulk SiC wafers has greatly improved and investigation of defect evolution without an epilayer could contribute to the feasibility of substrates for device processing. In this study, 100 mm n^+ 4H-SiC wafers were implanted with a single dose of $1x10^{15}$ cm^{-2} 60 keV Al^+ ions at varying implant temperatures from 400-700^{o}C. SIMS profiles are consistent with TRIM simulations demonstrating a gaussian dopant profile with an estimated FWHM of 55 nm. Samples were then coated with a protective cap and annealed in an induction furnace from 1650-1950^{o}C for 30 minutes to investigate extended defect evolution. Additional samples were laser annealed with two pulsed 532 nm Nd:YAG solid state lasers up to a fluence of $1.1\frac{J}{cm^2}$ and pulse length of 32 ns. Defects were examined using cross-sectional, plan-view, and dark-field TEM to identify different sub-threshold implant induced defects and to quantify their size and density. It was found that two types of extended defects formed upon furnace annealing—basal plane stacking faults and hexagonal shaped defects. Both defects coarsen with increasing annealing temperature up to 1950^{o}C. At 1950^{o}C, the hexagonal shaped defects disappear, potentially due to an increase in solubility, suggesting these defects could be composed of Al^+. However, their composition and origin is contested as it has been reported that basal plane dislocations and stacking faults are limited to Si and C interstitials, not implant species and this will be discussed. The experimentally observed defects could contribute to poor activation efficiency of Al^+ in SiC which will be debated using Hall Effect measurements. As basal plane dislocations and stacking faults have been shown to be composed of Si and C interstitials, the role of the protective carbon cap on extended defect formation and evolution and the SiC surface will be included. Due to the potential for constant C interstitial injection and low migration energy, the protective cap can greatly impact the size and evolution of these defects and the morphology of the SiC surface which has not been widely studied. Results from isochronal furnace anneals will be the focus of this talk, though, a comparison of the laser annealed samples on extended defect formation will also be presented.

Comparison of Annealing Quality after 3e15/cm² 50keV BF_2^+ implant between Rapid Thermal Annealing and Furnace Annealing

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Low leakage diodes are necessary in order to manufacture high quality variable capacitance diodes (varicaps), which are used in voltage-controlled oscillators. Junction leakage current affects the single sideband noise of the oscillator by up-conversion of 1/f and shot noise [1]. Several sources show higher leakage current for RTA compared to furnace anneal [2,3]. In our experiments we found lower leakage currents for RTA compared to furnace annealing. We presented results from annealing experiments where we compared six annealing conditions. Substrate is a 200 mm ntype silicon epi-wafers, 0.02 Ωcm bulk resistivity, with an epitaxial grown, 1e15 cm^{-3} phosphorus-doped layer. As a demonstration vehicle we fabricated p-n diodes as circles with varying radii and a p+ guard ring to suppress diffusion leakage currents as depicted in Figure 1. The annealing conditions to identify the effect on the leakage of the diodes are listed in the table below. We investigated junction properties with respect to leakage current from area and perimeter contribution, SIMS-profiles and crosssectional high- resolution TEM. In order to avoid influence of EOR which can produce excess diode leakage current from generationrecombination centers we annealed one sample with higher thermal budget by using RTA to achieve a deeper junction. A preliminary overview of the measured leakage current for the different annealing conditions is shown in Figure 2.

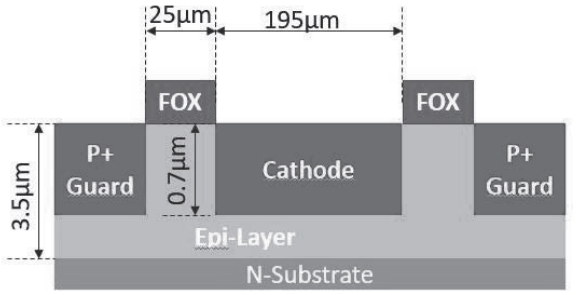

Figure 1: Cross section of the diode used for experiments

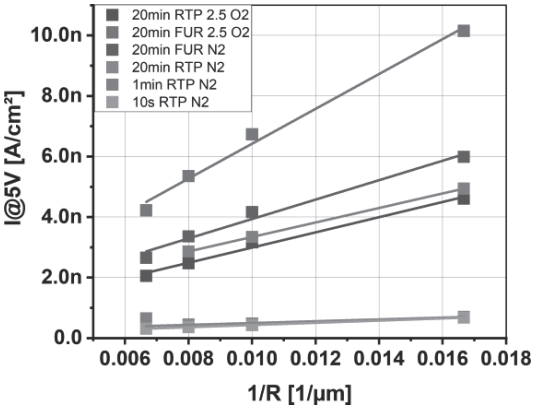

Figure 2: Junction leakage current density versus bias for A) RTA 1000°C 20min, B) RTA 1000°C 25min, C) RTA 1000°C 15 min + furnace, D) 1000°C 20min furnace

Split	I leak@5V	Leak Perimeter	Leak Area
	nA/cm²	nA/cm²	nA/cm²
1; 25min O2 2.5% RTP	0.789		
2; 20min O2 2.5% RTP	0.998	576	0.661
3; 10s N2% RTP	0.64	36.4	0.069
4; 1min N2 2.5% RTP	4.73	239.5	0.948
5; 20 min N2 RTP	0.473	30.0	0.199
6; 15min O2 2.5% RTP 1min O2 2.5% FUR	1.97		
7; 20 min O2 2.5% FUR	1.38	321	0.727
8; 20 min N2 FUR	3.6	251	0.482

References

[1] Chan, Y.-J., Huang, C.-F., Wu, C.-C., Chen, C.-H. et al., "Performance Consideration of MOS and Junction Diodes for Varactor Application," *IEEE Trans. Electron Devices* 54(9):2570–2573, 2007, doi:10.1109/TED.2007.903201.

[2] Lunnon, M.E., "Furnace and Rapid Thermal Annealing of P+/n Junctions in BF2+-Implanted Silicon," *J. Electrochem. Soc.* 132(10):2473, 1985, doi:10.1149/1.2113602.

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The Examination of Source Life and Beam Parameters of Germanium Implantation Using Hydrogen Carrier Gas

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I. Introduction

In the semiconductor industry, Germanium Tetrafluoride (GeF_4) has been the prominent source material for pre-amorphous (PAI) implants and it has posed major challenges to the industry due to several negative effects on the beam performance and source lifetime. The presence of H_2 helps to improve the source life. In the most recent development, implanter OEM, Axcelis has introduced H_2 generator which converts water (H_2O) to H_2 by electrolysis process. In this paper, the source performance of a Ge implanter using various source materials are evaluated and the optimum H_2 gas flow for H_2 generator was determined

II. Experiment

Three test runs were conducted in an Axcelis GSD200EE high current implanter equipped with a source assembly where all internal components are made from tungsten. These runs are conducted using different source materials as shown in Table I. For the H_2 generator, H_2 gas flow of 0.2 sccm was maintained. Each test is a marathon run with an accumulated dose measured at 3.5E+17 per day until source failure is encountered. This duration is recorded as source life. All source and beam parameters were monitored and recorded in the implant datalog. For the evaluation of the optimum carrier gas flow, the H_2 gas flow was adjusted as follows: 0, 0.16, 0.2, 0.3, 0.5, 0.7 and 1.0 sccm while the Ge gas flow was maintained at 2.4 sccm. Under each condition, implantation was performed and arc current was recorded for comparison purposes, in order to determine the most optimum H_2 gas flow.

III. Results and Discussion

TABLE I. Result Comparisons

Test	Condition	Source Life	Failure Mode
i	GeF_4 gas bottle	7 days	Cathode & repeller coated
ii	GeF_4 pre-mixed H_2 gas bottle	10 days	Bushing coated
iii	GeF_4 gas bottle with H_2 generator	17 days	Bushing coated

A. Visual inspection

It was observed that heavy coatings were formed on the tungsten liner in the arc chamber, cathode and repeller for test (i). Metal whiskers grown on the cathode and repeller were about 5mm thick. For test (ii), the coating on the arc chamber liner was thinner. Source from test (iii) was observed to be the cleanest, with nearly negligible coating. Source from test (iii) would have lasted longer if not for the heavily coated bushing that caused extraction arcing events.

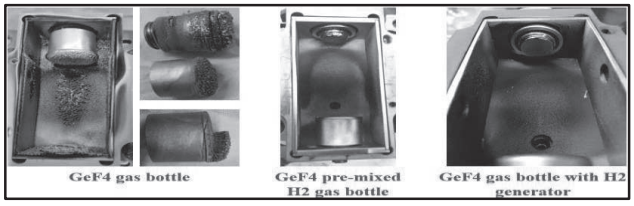

Fig. 1. Arc chamber comparison for different conditions

B. Source parameters comparison

The arc current and Germanium gas flow required to get the given source beam was lowest for GeF_4 gas bottle with H_2 generator, followed by premixed GeF_4 and H_2 gas bottle and pure GeF_4 gas bottle. Moreover, the implementation of GeF_4 gas bottle with H_2 generator had been observed to have the lowest filament current and cathode current to generate the same amount of Ge+ ions. The source magnet current was also observed to be lowest and more repeatable on the GeF_4 gas bottle with H_2 generator due to the better ionization efficiency and beam stability. Furthermore, the extraction current of using a GeF_4 gas bottle with an H_2 generator was the lowest as compared to another source material type due to its better ionization efficiency and the amount of coating at the arc slit was minimal. Thus, ions could be extracted easily with minimum extraction current.

C. Effect of different H_2 gas flow supplied by the H_2 generator

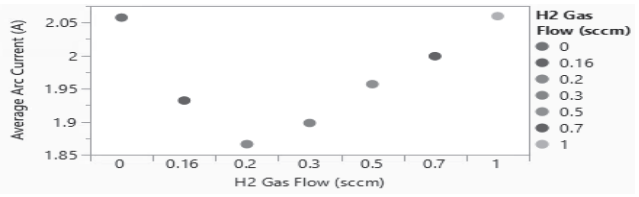

Fig. 2. Arc current of different H_2 gas flow

As shown in Fig.2, the arc current increased when the H_2 gas flow increased because the ratio of H_2:GeF_4 gas in the arc chamber is higher. This hinders the ability of the source to maximize the number of Ge+ ions produced. Thus, a higher arc current is needed to achieve the desired source beam. However, low H_2 gas flow resulted in higher arc current due to insufficient H_2 molecules to combine with the fluorine ions. The 0 sccm H_2 flow is just equivalent to GeF_4 without H_2. In conclusion, the optimum H_2 gas flow is 0.2 sccm which yields the best ionization efficiency.

Where is the Annealing Technology Going for Better Device Performance?

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Annealing technology has been mainly discussed on electrical activation of ion implanted impurity atoms in semiconductors and annihilation of defects caused by ion implantation or secondary defects after annealing. From the viewpoint of electrical activation, higher temperature and ultra-short duration annealing is better for achieving higher electrical activation. Ultra-shallow pn junction is also required in semiconductor devices. The advantage of ultra-shallow junctions for the source/drain extensions with lower resistance is to improve short channel effects and to reduce parasitic resistance in high performance MOSFETs leading to smaller RC delay.

When rapid thermal anneal (RTA) of typical annealing length is 1-3 sec is used, we confront the trade-off problem between thermal diffusion of dopant atoms and the electrical activation, which is limited by the solid solubility of impurity atoms. Therefore, RTA is required to suppress impurity diffusion while maintaining the electrical activity. In this respect, higher temperature and shorter annealing time as short as several 10 nsec to several 10 msec. As a result, nanosecond annealing (NSA) and millisecond annealing (MSA) are widely applied to ultra-shallow junctions in semiconductor manufacturing.

On the other hand, defect annihilation takes more time than electrical activation. This requirement is essential in deep source and drain with higher impurity concentration, i.e., higher ion implantation dose. Heavy dose ion implantation damage can be partly solved by raised source and drain (S/D). However, implantation damage problem still remains. If the annealing length becomes longer, the diffusion length of impurity atoms becomes longer and can cause short channel effect and threshold voltage deviation. Therefore, MSA and NSA is also required to reduce dislocation density so that the p-n junction leakage can satisfy the device requirement for high performance MOSFETs. Or the formation of the deep S/D needs to be followed by extension formation process.

Another important thing is to suppress the deactivation of impurity atoms. The deactivation of impurity atoms occurs because multiple annealing cycles are necessary for the device. In the case of the lower temperature annealing is carried out after NSA or MSA, substitutional site impurity atoms segregates during 600-900 ^{o}C annealing. This phenomenon is very natural considering the solid solubility of impurity atoms in semiconductors. Hydrogen passivation sometimes degrades electrical activation of B and P in Si. On the other hand, hydrogen atoms can terminate Si dangling bonds and reduces interface states at the SiO_2/Si interface and fixed charge in a gate oxide. Therefore, we need to keep company with hydrogen and can do fine if we optimize the annealing conditions.

In this paper the compartmentalization of wide variety of annealing and the combination are discussed on the viewpoint of total process integration in order to achieve better device performance.

Photoluminescence characterization of He-implanted SiC upon nanosecond laser thermal annealing.

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Silicon carbide (SiC) has been demonstrated to be a promising material for the implementation of quantum technologies devices, mainly due to its wide bandgap such as other semiconductors like diamond, its highly remarkable physical properties (thermal conductivity, electron mobility…[1]) and the availability of luminescent defects emitting in the telecom wavelength range.

An important challenge towards its widespread uptake of practical applications in the field of quantum technologies, is the identification of a fabrication method for the color centers in SiC, that ensures optimal optical performance and paves the way towards a more deterministic activation of individual dopants emitters.

On the basis of this goal and preliminary successful results on laser writing [2], along with several studies showing the ablation and behavior of the nanosecond laser on SiC [3]; this work demonstrates the viability μm-sized, focused laser-induced thermal processing for the local activation of optically centers subsequently to ion irradiation process. This approach could provide a more effective method with respect to consolidated homogeneous thermal annealing processes for diffusion of the crystal lattice vacancies, both recovering the pristine structure and promoting the formation of stable defects.

We report on the photoluminescence characterization at ensemble level of high-purity 4H-SiC samples irradiated with 1 MeV He+ ions and processed with different laser-induced annealing schemes performed. Particularly, we report on the investigation of the effects of ns-pulsed processing in the parameters space of laser wavelength (532 nm and 355 nm) and instantaneous power, to identify the role of each in the formation of optically active color centers.

A systematic Raman analysis, along with single-photon sensitive confocal microscopy photoluminescence characterization have been carried out to identify the role of optical beams with energies above and below the energy gap of the material, respectively, and to compare the resulting activation efficiencies with samples processed under conventional homogeneous thermal annealing processes.

The results achieved in this show a promising technical pathway towards the fabrication of VSi centers in SiC under controlled, local conditions with the potential for uptake in large-scale manufacturing processes.

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Thermal Budget Reduction for Spike Anneals in Conventional RTP

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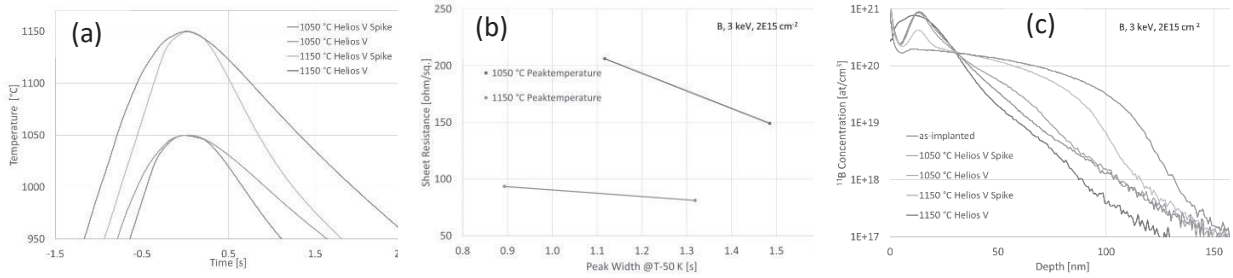
Thermal budget reduction in rapid thermal processing (RTP) has been a requirement since the beginning. In this paper we will focus on the spike anneal thermal budget reduction by means of decreasing the time at 50 K below peak temperature. This time $t_{T\text{-}50K}$ is referred to as peak width at T-50 K [1,2]. Wafer cooling through conduction and convection can be increased via addition of 1.5 slm Helium to N_2 reducing the peak-width from >2 s to 1.4 s for a 1090 °C spike anneal [1,2].

In this work we investigated the activation and diffusion behavior of a 3 keV, 2E15 cm^{-2} Boron implant which was annealed on both, a standard Helios® V RTP system and a Helios® V spike system with enhanced spike anneal sharpness. Peak temperatures investigated were 1050 °C and 1150 °C. Those two processes were compared with respect to activation and diffusion. In contrast to the standard Helios® V configuration, the tool with enhanced spike performance uses special temperature controller settings and a 'high absorptive lamp field'. Sharper spike-anneal temperature profiles originate from: (i) improved controller settings mainly influencing the 'ramp-up slope' and (ii) enhanced radiative wafer cooling *after* peak temperature due to *increased* absorption of the thermal radiation emitted from wafer and lamps. Since thermal radiation follows the Stefan-Boltzmann-Law and is proportional to ~T^4, the benefit from the 'high absorptive lamp field' is most pronounced at elevated temperatures. In (a) temperature profiles for 1050 & 1150 °C spike anneals are compared. For 1150 °C peak temperature, peak width @ T-50 K can be reduced by 32%, from ~1.3 s to ~0.9 s, while at 1050 °C peak temperature, peak width is reduced by 25%, from 1.5 s to 1.1 s (b).



(a) Temperature Profile Comparison between Standard Helios® V tool and Helios® V Spike tool; (b) Sheet Resistance – Peak Width Correlation for 1050 & 1150 °C; (c) SIMS Profiles for 1050 & 1150 °C.

Due to smaller peak width, sheet resistance is increased by 38% (b), whereas junction depth determined at a concentration of 1E19 cm^{-3} decreases by 10% at a peak temperature of 1050 °C (c). Despite the lower sensitivity of the implant at the higher process temperature of 1150 °C (b), sheet resistance is higher by 15% (b) and junction depth is smaller by 15% (c).

Combining improved temperature controller parameters and a high absorptivity lamp field, the new Helios® V Spike system enhances spike anneal sharpness yielding 30% peak width reduction and 15% junction depth reduction for the investigated B implant condition (3 keV, 2E15 cm^{-2}).

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Nanosecond Pulsed Laser Activation of Phosphorus in Germanium

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Since the industry demands information technology (IT) progress, the technology node of transistors touched 10 nm, and we must exceed silicon and move to higher mobility channels such as germanium. Germanium has the most increased hole and electron mobility, low processing temperature, and high density of states for carriers. Despite all the advantages, germanium suffers from its poor quality of n-type doping at the source/drain area. In this work, the nanosecond laser was applied to activate ion-implanted phosphorus and minimize dopant channeling issues in germanium.

Phosphorus was implanted with a dose of $1\times10^{16}/cm^2$ into (100) germanium at the energy of 15 keV to optimize the thickness of an amorphized layer. Before pulsed laser activation, a 100 nm thick SiO_2 layer was deposited as a capping layer. Pulsed laser activation was performed by a 355 nm Nd:YAG laser with a repetition frequency of 70 kHz and a pulse duration of 30 ns. The energy density was controlled while the scanning speed was fixed to 1 mm/s. The gaussian laser beam was shaped into a Top-Hat line beam to apply laser annealing uniformly. The capping layer was removed after pulsed laser activation.

Recrystallized layer after pulsed laser activation was observed by cross-sectional transmission electron microscopy (TEM) and fast Fourier transformation. We chose the three representative states, 75 mJ/cm^2 for a low laser energy density that the implanted layer is still amorphous, 120 mJ/cm^2 for a moderate energy density that implanted layer was recrystallized and the substrate is still crystalline, and 250 mJ/cm^2 for a too high energy density that the substrate is also melted losing crystallinity. Dopant profiles, with the highest concentration of $1\times10^{21}/cm^3$, were obtained by secondary ion mass spectrometry (SIMS) with depth profiling. Carrier concentration was obtained by Hall effect measurement, and it reached $3.26\times10^{20}/cm^3$. With the optimized processes, diffusion of dopants was successfully suppressed during the activation process. We used the four-point probe method for sheet resistance measurement for electrical analysis. As a result, the laser energy density of 120 mJ/cm^2 showed the lowest sheet resistance of 2.48 Ω/□ while 75 mJ/cm^2 and 250 mJ/cm^2 were measured as 2.98 Ω/□ 3.01 Ω/□ each. Lastly, I-V characteristics of gold (Au) contacts to germanium as a function of the energy density of laser annealing are measured. The energy density of 140 mJ/cm^2 showed the best contact behavior with the ohmic trend. In conclusion, the optimization of pulsed laser annealing on recrystallization and activation with suppressed dopant diffusion allowed to form of low resistive source/drain contacts on germanium.

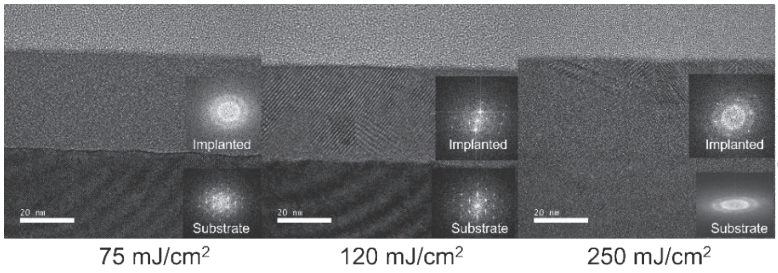

Figure 1

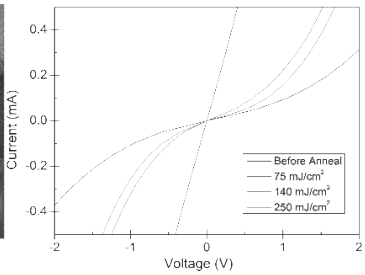

Figure 2

Acknowledgment

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Laser Annealing Applications for Advanced FinFETs and Beyond

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Advanced CMOS transistors with 3-D channels achieved a significant reduction in the channel resistance per footprint making the external resistance a performance limiter. Short-duration laser annealing techniques provided knobs for reducing various components of the external resistance and have been adopted in CMOS manufacturing. This invited presentation reviews applications of sub-millisecond laser annealing for advanced FinFET transistors and outlines further performance improvements by employing nanosecond-scale laser annealing. The continuing trend of decreasing transistor channel resistance per footprint will put even higher focus on reducing its external resistance in the future. Doping and non-equilibrium activation techniques such as laser annealing will continue to play an important role in balancing out external and channel resistances.

Ion Implantation Isolation for GaN HEMT: Mechanism and Parasitic Effects

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Ion implantation has been a widely applied isolation technique for wide bandgap semiconductors. Comprehensive knowledge of the exact mechanism of ion implantation isolation for GaN HEMTs provides guidance for further refinement of the technique. In a recent study [1], we find that the sheet resistance R_{sh} of the isolation region—a key indicator of isolation quality—is determined by an interplay between net polarization charges in GaN heterostructures and the point defects generated by ion implantation. This explains why the R_{sh} of isolation regions depends only weakly on ion species but strongly on post-isolation thermal budget [1-6] (Fig. 1). The isolation and leakage mechanisms of ion implantation isolated GaN heterostructures [1] can be understood by introducing native point defect with specific energy levels [7] into the energy band diagram (Fig. 2).

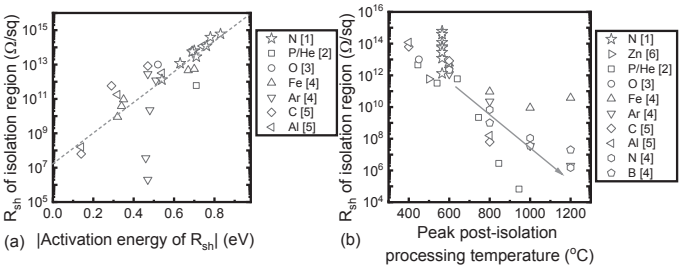

Fig. 1 Benchmarks of R_{sh} of ion implantion isolated AlGaN/(AlN/)GaN heterostructures as a function of (a) activation energy of R_{sh} and (b) post-isolation processing temperature. Dashed line in (a) reflects a common mechanism behind the R_{sh}. Arrow in (b) indicates abrupt reduction of R_{sh} with heating from >600°C processing.

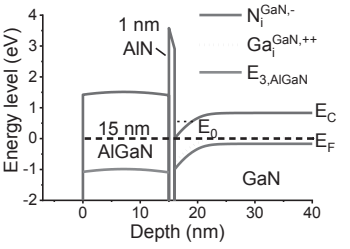

Fig. 2 Knowledge of point defects-based isolation mechanism in GaN heterostructures guides construction of energy band diagrams for isolation regions.

High-quality isolation is guaranteed by a large amount of native defects generated by ion implantation. However, a part of ions penetrate laterally into the active channel and cause parasitic device behaviour. The lateral ion penetration and point defect generation are visualized by 2D TRIM simulation [8] (Fig. 3). We extract from experiments the characteristics of the parasitic channels at the sides of the devices (Fig. 4), which could be well described by an reduced effective device width (W_{eff}) compared to the nominal one W_{nom} (Fig. 3, Fig. 4). These parasitic effects are theoretically understood combining the knowledge gained from the ion implantation isolation mechanism.

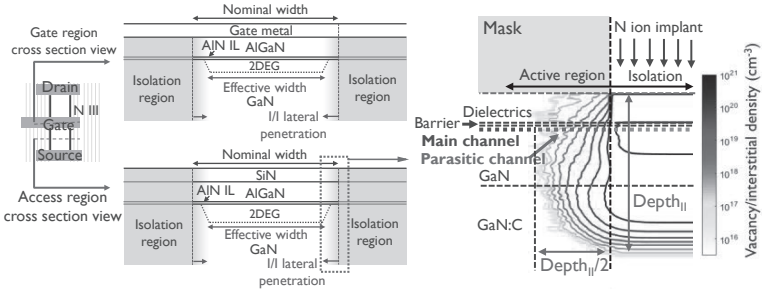

Fig. 3 Schematics of GaN HEMT cross sections and 2D SRIM simulation showing that parasitic channels form at the sides of GaN HEMT due to point defects generated by lateral penetrated implanted ions. The parasitic channel width is close to half of the implantation depth.

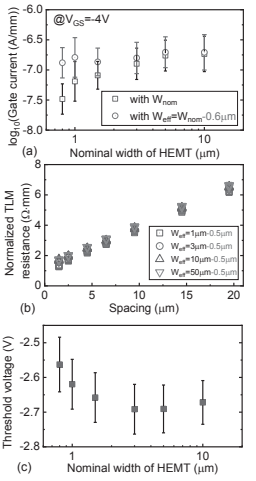

Fig. 4 Comparison of devices with varied widths suggest parasitic side channels formed by lateral ion penetration have (a) reduced gate current, (b) reduced conductance, and (c) increased threshold voltage.

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Characterization of structural defects induced by heated implantations and annealing process

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Leakage current in CMOS devices is known to increase in presence of various types of interstitial structural defects such as small interstitial clusters, {311} rod-like defects or dislocation loops. Heated implantation enhances interstitials and vacancies recombination and thus reduces the damage caused by the implantation. Such reduction of the amount of interstitials is crucially important for a correct prediction of the subsequent formation of extended defects. On the other hand, heated implantations can result in the formation of more stable interstitial clusters (compared to those formed during a RT implant), which may therefore dissolve at a slower rate during the subsequent annealing sequence. Heated implantation thus results in two competing phenomena in a way that the final outcome strongly depends on the precise experimental conditions.

In this paper the residual defect type and concentration induced by a process combining heated implantation and an industrial annealing sequence is investigated (peak temperature: 800 °C). Arsenic implantations have been performed at Room Temperature (RT), 150 °C and 500 °C. The implanted wafers have been subsequently annealed using the same annealing sequence. The damage level in the as-implanted samples was investigated by TEM cross-section images. Similarly, the presence of extended defects after the annealing sequence has been investigated by TEM images in cross-section and plan-view. Photoluminescence (PL) spectroscopy has also been used to investigate the presence of smaller clusters with sizes below the TEM detection limit.

The heating effect on the as-implanted damage is clearly highlighted in the TEM images of the as-implanted wafers. In the RT case the implantation results in the formation of a continuous amorphous layer (bright area on Fig. 1. A), whereas, in the 150 °C and 500 °C case, no amorphous layer is formed (Fig. 1.B and 1.C).

After the annealing sequence, extended defects are observed in all the wafers. The RT and 150 °C implantations both exhibit dislocation loops after the annealing. In the 500 °C implantations case {311} defects are observed in the TEM plan-view images (no dislocation loops). A count of the interstitials trapped in the defects observed in TEM is presented in Table 1. The RT and 150°C have a close number of interstitials trapped in loops whereas considerably fewer interstitials are trapped in the {311} defects observed in the 500 °C case.

The RT and 150°C implanted wafers exhibit a similar behavior also in the PL spectra. In these two implantations two broad peaks are observed near 1300 nm (A1-A2 in RT and A3-A4 150°C in Fig. 2). The evolution of the PL spectra depending on the PL acquisition temperature (not shown here) also demonstrate same trends between A1 and A3 and A2 and A4 and suggest that these peaks are associated to the same defect type. Similar peaks have been reported in literature in the presence of small interstitial clusters. The PL peaks of the 500 °C implantation are different from the ones observed in the RT and 150 °C cases. The PL signal of the 500 °C implantation is composed of several peaks between 1140 and 1400 nm. A clear identification of peaks wavelength and broadening is difficult in this case because of the overlapping between them. Additional annealing steps at higher temperature are expected to further modify the observed PL peaks and help identifying their origin. In addition to the initial annealing sequence, the 3 wafers have therefore been annealed at 4 temperatures (700 °C, 800 °C, 900 °C and 1000 °C) for 30 minutes. PL experiments are currently performed and results will be reported in the full paper.

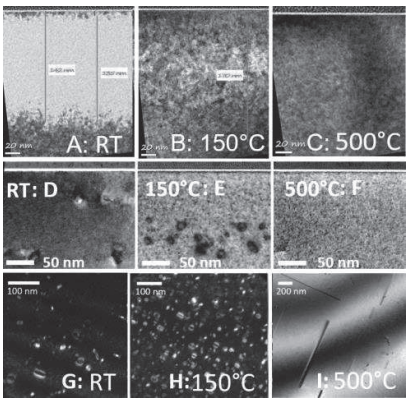

Figure 1: TEM images of the wafers (Top) as implanted in cross-section (Middle) annealed in cross section (Bottom) annealed in plane view

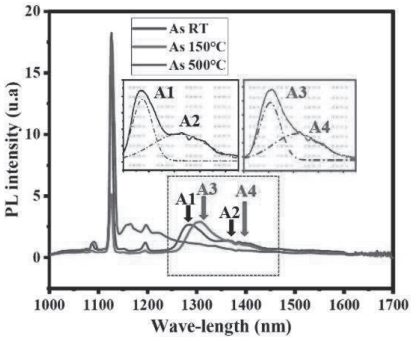

Figure 2: PL spectra of the RT, 150°C and 500°C implanted wafers after the annealing

Implant temperature	RT	150 °C	500 °C
I density (cm^{-2})	$1.4\ 10^{14}$	$1.6\ 10^{14}$	$5.1\ 10^{12}$

Table 1: Densities of interstitials trapped in the defects observed in TEM for the 3 implantations

Ion Implantation Technology in SiC for Advanced Electron Devices

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SiC has received increasing attention for high-power and high-temperature devices, which outperform the Si counterparts. Availability of successful ion implantation of both n- and p-type dopants in SiC offers much flexibility in device design, enabling to significantly improve the performance and reliability of SiC devices. In recent years, ion implantation technology in SiC has been upgraded to an advanced stage, where new technological challenges emerge. In this paper, two subjects mainly investigated in the authors' group associated with ion implantation technology in SiC are reviewed.

Formation of a heavily-doped region by ion implantation is a key for achieving a low contact resistivity of ohmic contacts. This is especially critical in SiC, because the barrier height of metal/SiC junction is high due to its wide bandgap. The authors conducted P^+ ion implantation into n-type SiC epilayers to form a box profile (P atom concentration: $1x10^{17}$ – $1x10^{20}$ cm^{-3}). Post-implantation annealing was performed at 1750°C for 20 min in Ar with a carbon cap. Figure 1 shows the net donor concentration obtained by *C*–*V* measurements on Ni/SiC structures vs. the implanted P atom concentration. Nearly perfect (> 98%) activation of implanted P atoms was achieved even for a very high doping concentration over 10^{19} cm^{-3}. The *I*–*V* characteristics of Schottky structures with several different metals formed on heavily-doped SiC (without contact sintering) were investigated. Analyses of the current taking account of tunneling through the Schottky barrier revealed that the current density of the Schottky structures on SiC formed by high-dose P^+ implantation is higher than that on heavily-doped epitaxial layers by several orders of magnitude at a given donor concentration, which can be ascribed to trap-assisted tunneling originating from implantation-induced damage. This trap-assisted tunneling is beneficial for formation of ohmic contacts without contact sintering at high temperature (> 950°C) that is commonly adopted in the SiC community.

The authors proposed a complementary JFET (CJFET) device for ICs operational in harsh environment (high temperature, radiation). Since high-purity semi-insulating (HPSI) SiC wafers with a resistivity over 10^{12} Ωcm (at 300 K) are available, SiC CJFETs can be fabricated simply by several ion-implantation steps into a HPSI SiC wafer without a complicated device isolation process. Figure 2 illustrates a schematic structure of a SiC CJFET fabricated on a HPSI substrate. The double-gate structure formed at the both sides of the channel region easily enables normally-off operation that is required for CJFET operation. In this study, SiC CJFET logic gates were assembled by the ion-implantation-based p- and n-JFETs. The doping concentration of the gate and channel regions were $5x10^{19}$ and $5x10^{16}$ cm^{-3}, respectively. From the transfer characteristics of the p- and n-JFETs, threshold voltages of the p- and n-JFETs were determined as −0.63 and 0.61 V (normally-off), respectively. Operation of SiC CJFET-inverter and NOR gate at 350°C was demonstrated with a single and low supply voltage (V_{dd}) of 1.4 V. Degradation of the output voltage was within the instrumental error (less than 1%) even after 750-h operation at 573 K.

This work was supported in part by the OPERA Program from the JST and the JSPS KAKENHI (# 21H05003).

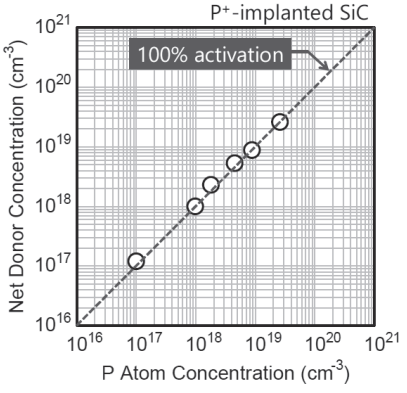

Fig. 1: Net donor concentration vs. implanted P atom concentration in SiC.

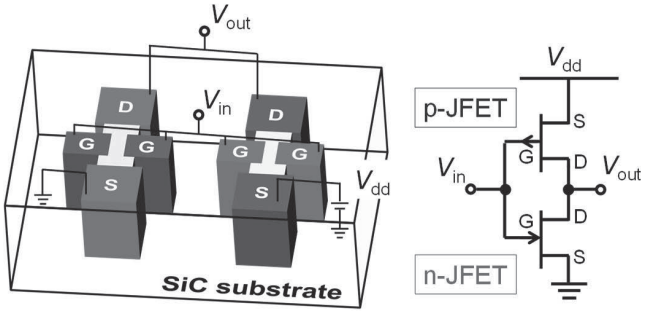

Fig. 2: Schematic structure of a SiC CJFET and inverter circuit diagram.

Advanced Angle Control Requirements and Solutions for Enabling High Aspect Ratio Device Structures

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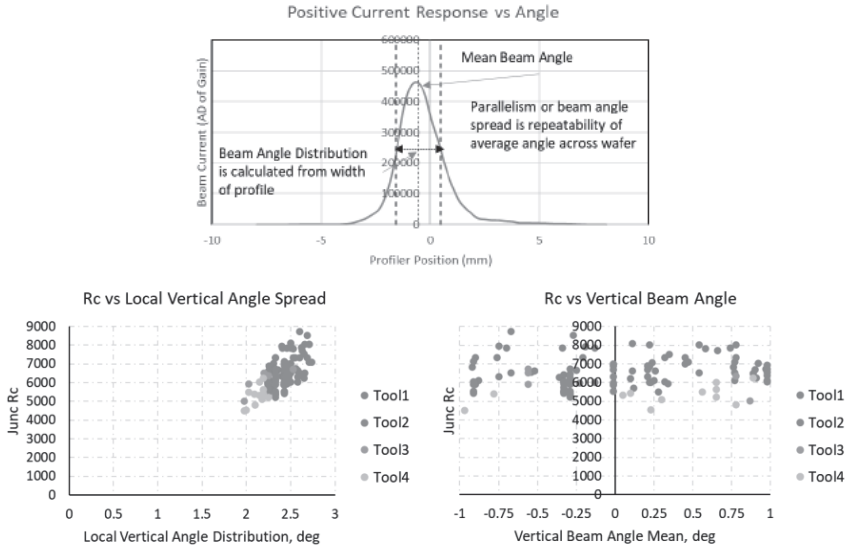
Abstract – Process variation within-wafer and from batch-to-batch presents a significant challenge for manufacturing DRAM devices constructed with high aspect ratio architectures. One specific challenge in manufacturing such devices arises from the difficulty in uniformly doping contacts when low energy ions must be implanted through high aspect ratio holes. Conventional methods of measuring the average incidence angle of the ion beam relative to the axis of the hole are insufficient to deliver acceptable levels of dopant uniformity. While all modern ion implanters measure and control the average incidence angle of the beam or beamlet to the wafer at several points representatives of the total wafer area, the local distribution of angles within the local region of the beam becomes non-trivial with decreasing ion energy and increasing ion current simply from the physics of beam transport.

Due to this consideration the proportion of ions reaching the contact at the bottom of the hole for low energy implants is sensitive not only to the average incidence angle but also the local distribution of angles and the forward scattering probability of an ion off the device sidewall. This paper describes the device manufacturing challenges; the model developed to motivate the investigation of next generation angle quality measurements. The methods co-developed by SK Hynix and Axcelis to measure, interlock upon and independently tune average incidence angle and local angle distribution on a high current scanned spot beam system are explained.

Finally, a comparison is then provided to demonstrate the superior uniformity and repeatability achieved on high aspect ratio devices when these advanced process control capabilities are applied relative to conventional capabilities.



Figures: getting incidence angle and angle distribution from raw current measurement and demonstration that Rc for high aspect ratio structures are more sensitive to the local angle distribution than the mean beam angle.

Precise Angle Control for Channeling in SS-UHE, Single Wafer Ultra-High Energy Ion Implanter

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In recent years, deeper photodiode (PD) structures in advanced image sensors have been pursued to obtain higher light sensitivity. In order to form a deep PD structure, ultra-high energy implantation is required. For example, at least 4 MeV Phosphorus implantation is required to form a PD with depth of 3 μm or deeper with a "random" beam incidence angle. More than 3 MeV Boron is required for the cell isolation as well. Therefore, the required masking photoresist should be thick enough to stop high energy ions, leading to a significantly high aspect ratio, up to 30 or more. Reliable near-zero angle implantation should be provided for effective implantation into these deep diode and trench structures.

It is well known that a strong dopant profile shift by the channeling effect is inevitable for the zero degree implant especially for the high energy implantation. In order to obtain a reliable dopant depth profile, implant angle accuracy should be secured. However, because the ion beam trajectory can be varied when the initial beam trajectory extracted from an ion source changes, this trajectory variation leads to angle variation which is not negligible for high energy implantation.

Sumitomo Heavy Industries Ion Technology's (SMIT) single-wafer ultra-high energy implanter, the SS-UHE, is designed to realize ion implantations with precise angle control with a unique technology, that is, a combination of the movable beam slit and beam profile monitor.

Boron implantation was performed at around zero degree with the SS-UHE into Si(100) wafers. The dopant depth profiles were measured by SIMS. Figure 1 shows the SIMS profiles with different tilt angles in 0.025° increments from 0.25° to 0.35°. The lower the tilt angle is, the deeper the SIMS profile is because the implant beam angle is precisely controlled. Figure 2 shows the SIMS profiles with the same condition as Figure 1, demonstrating machine-to- machine angular integrity in terms of the depth profiles measured by SIMS.

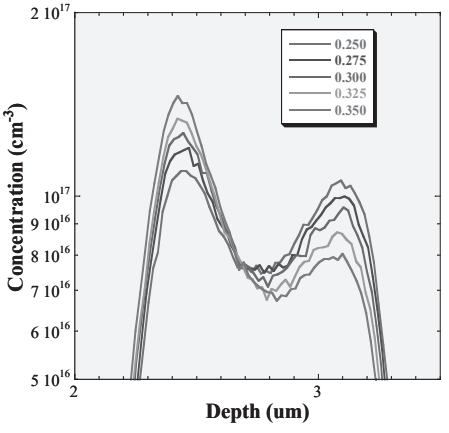

Fig. 1. Depth profile with the tilt angles of 0.25° to 0.35° by increments by 0.025° with 1.5MeV Boron at 1E13 atoms/cm^2 implantation.

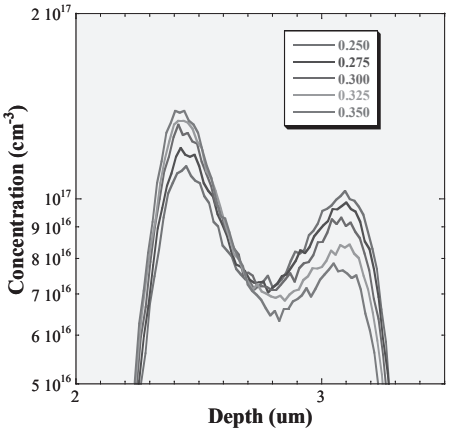

Fig. 2. The same depth profile data as Fig.1 with a different tool to demonstrate the machine-to-machine beam incidence angular control.

PMOS Rc reduction using B_2H_6 plasma doping process for current and next gen DRAM devices

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As CMOS technology in DRAM becomes more logic-like, the requirement to enhance performance is increasingly critical. In the CMOS devices in peripheral circuit, scaling has brought the gate to contact spacing to a tight critical dimension. This enhances the difficulty of device makers to reduce contact resistance (Rc), to improve short channel effect (SCE) and increase drive current (Ids). Furthermore, the contact size and critical dimension scaling requires a uniform and high concentration dopant to meet the Rc, leakage and Ids requirements. Boron doping via the use of B2H6 (diborane) PLAD has enabled device makers to improve the PMOS peripheral device performance for the current node and beyond. To achieve this, we identified a new process space and new hardware (H/W) that yield a higher B retained dose, with reduced net deposition, better uniformity, and increased productivity. In this work, we demonstrate validation of this "triple point" (device gain, uniformity improvement, productivity enhancement) achievement for device makers at the 16nm node by enabling high dose, near surface doping.

We characterized the boron process extensively using various in-situ and ex-situ techniques to gain fundamental understanding of the process and mapped out a process space to minimize deposition and enhance B ion fraction [1]. This new process enables high concentration B doping, which yields surface peak dopant profiles as shown in fig. 1 and is critical to lowering Rc. Additionally, we have also developed a new hardware (H/W) solution that allows further deposition control and increased dopant retention, resulting in significant Rc reduction as well as better within wafer uniformity. Initial B dose retention studies were performed using SIMS and Rs measurements (fig. 2), whereas Rc improvement (fig. 3) was validated using a contact chain test structure. The combination of the newly identified process space and new H/W allows DRAM chipmakers a highly differentiated solution to improve Rc, uniformity, device performance and yield as well as node over node sustainability. The new H/W solution and the optimized B2H6 process are currently being evaluated by DRAM manufacturers for adoption in next node and initial results show substantial improvement in device performance.

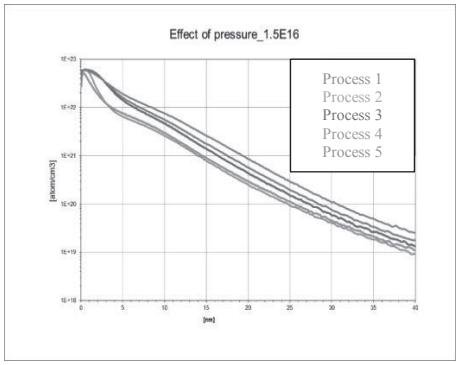

Fig. 1 B SIMS vs process variable

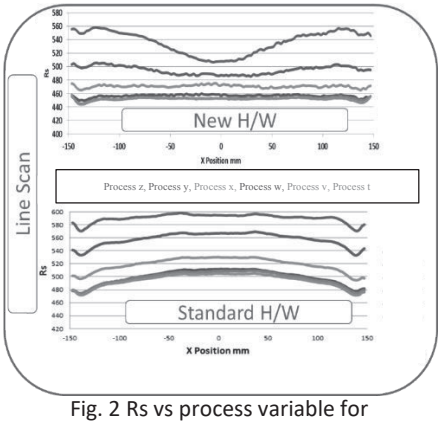

Fig. 2 Rs vs process variable for different H/W

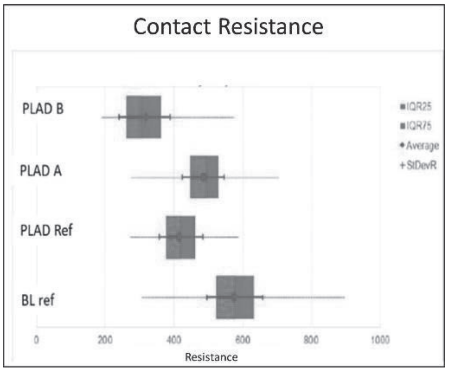

Fig. 3 Rc validation for new H/W and process using contact chain lot

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New ECR Ion Implanter with Advanced Wafer Temperature Control

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Ion implanters for substrate engineering (e.g. “smart-cut” wafer cleaving via blister formation [1]) require careful control of the implant temperature. Blister formation is discussed for Si, SiC, AlN, GaN, & GaAs substrates. Most materials implanted in this application space require implant temperatures well above room temperature for optimum blister formation [2], with a maximum before destructive blisters form prematurely. Temperamental materials have a “goldilocks” implant landscape, too hot or too cold results in the total lack of blisters [3].

A new high current H/He ion implanter utilizing an ECR ion source accelerator [4] with high frequency XY magnetic scanning is presented [5]. Proton currents of 60mA (upgradable to 100mA) are achieved with ion energies of 130kV (upgradable to 300kV) [6]. Some advantages of the ECR source are fast beam setups, high currents, and minimal maintenance. No source changes or accelerator maintenance were performed in a six-month period. Over 800 successful implants were performed in a period of a year with no source changes.

Implant substrate temperature data is shown via thermocouples and real-time FLIR cameras [7] that capture the surface wafer temperature excursions. Figure 1 below displays a picture frame from a video of the real-time FLIR data obtained as a wafer is implanted with 60mA of protons at 130kV. Real-time feedback control limits temperature excursions and controls wafer backside gas cooling to an optimum set point.

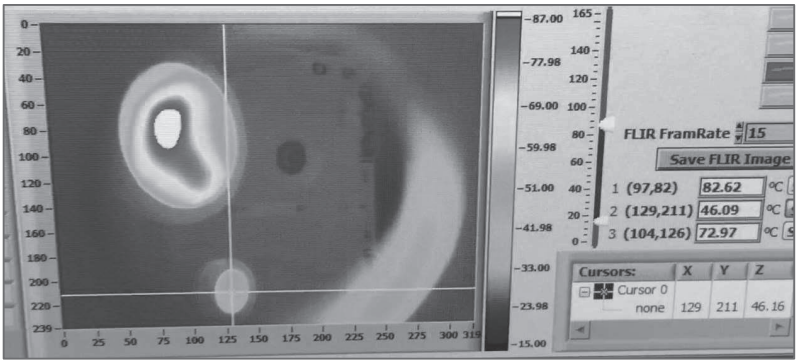

Figure 1: Real-time wafer surface temperature monitoring with a FLIR camera

The heat load is controlled via the high-speed magnetic scanning of the high intensity 60mA ion beams, implant duty cycles, scan rates and the advanced wafer backside gas cooling. The end station has no moving parts resulting in exceptional particle performance. A dual end station maximizes beam utilization resulting in very high wafer throughputs from 50 to 300mm for high dose 5e16 implants. Non-regular or delicate wafers sizes or shapes can also be accommodated.

Introducing the Purion H200™, single wafer high current implanter designed to address unique high dose implant applications

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The growing market demand for semiconductor chips designed to address new and emerging applications (especially in the power device market) are driving the need for single wafer high current implanters with a much broader energy range than traditional implant space primarily designed around the logic and memory applications [1].

This paper describes the design and capabilities of the Purion H200™ single wafer high current implanter produced by Axcelis technologies specifically designed to deliver industry leading beam currents and productivity over a wide energy range from sub 10keV to over 400keV delivering an effective path for fabs to increase their output (wafer outs/m2) from the implant bay. Figure 1 shows the layout of the Purion H200 illustrating the high current beamline integrated with post acceleration architecture on the Purion single wafer handling platform. We discuss the design, capabilities, and unique challenges with higher power implants and review the current applications needs being addressed by this implanter in high volume manufacturing of both silicon and silicon carbide devices.

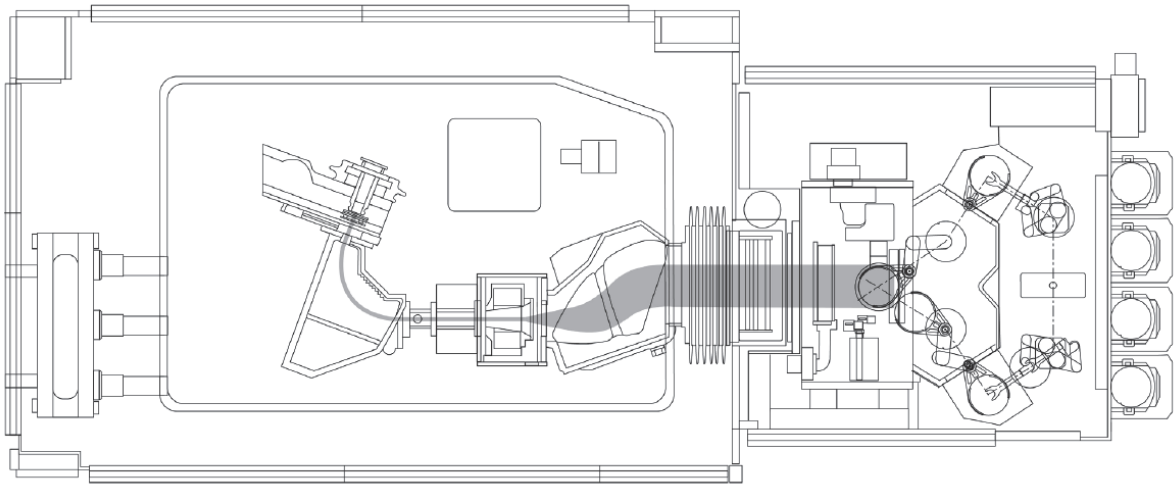

Figure 1 Purion H200 beamline layout.

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Flash lamp annealing of semiconductor materials

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Flash lamp annealing (FLA) is a non-equilibrium annealing method on the sub-second time scale which excellently meets the requirements of thin film processing. It has already been used in microelectronics, mostly after ion implantation, to activate dopants, to recrystallize amorphous semiconductor layers, and to anneal out defects. Another field of application is the formation of silicide and germanide materials for contact fabrication. However, in the last 20 years, FLA has opened up new areas of application like thin films on glass, sensors, printed electronics, flexible electronics, energy materials etc. Since two years, the Helmholtz Innovation blitzlab aims to transfer this technology to industry and application-related research.

After a short introduction, a brief overview to FLA is given, discussing the advantages and challenges of this technology. The main part displays various examples from literature and from own research, in which FLA has been applied to semiconductors, namely to Si, Ge and GaN. In detail, the formation of ultra-shallow junctions, the doping close or even above the solubility limit of dopants, the formation of NiGe for contacts, and p-type doping in GaN is addressed.

Influence of N doping on the Crystallization Kinetics of Phase Change Materials ($Ge_2Sb_2Te_5$)

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Abstract: Chalcogenide Ge-Sb-Te (GST) alloys are used in digital Phase Change Memories (PCM) where the bit of information is encoded in the resistivity of the material, high in the amorphous state, low in the crystalline state. These alloys are also foreseen as the materials of choice for fabricating neuromorphic devices able to mimic synaptic activity. However, their crystallization temperature, of about 140-170°C for the canonical $Ge_2Sb_2Te_5$, severely limits the application domains. N doping (up to few %) of the material during deposition has been reported to significantly improve its thermal stability. However, the origin, at the atomic scale, of this alteration remains unknown. One reason for this limited understanding lies in the difficulty to infer the mechanisms which are impacted by N during crystallization based on the sole observation of the microstructures found after annealing of a few N doped and undoped samples. For this reason, we have prepared specifically designed layers by combining deposition and ion implantation techniques and used a combination of in-situ and ex-situ transmission electron microscopy (TEM) techniques allowing us to image in real-time and compare the crystallization kinetics and characteristics of N-doped and undoped $Ge_2Sb_2Te_5$ during annealing in the TEM. Beyond evidencing that the crystallization temperature is higher in N doped regions, we have analyzed and compared the growth characteristics of the crystalline phase in relation with the doping level. We demonstrate that N renders the crystallization process more “nucleation dominated” (addition of small nuclei, reduced growth of existing crystals) which is ascribed to the increased viscosity and mechanical rigidity of the amorphous state caused by the formation of Ge–N bonds. At higher annealed temperatures, N hampers the coalescence of the crystalline grains, and the cubic to hexagonal phase transition. Making use of a recently invented TEM-based technique, we evidence that the nanocrystals formed from the crystallization of N-doped amorphous GST-225 are under tension, which suggests that N is inserted in the lattice and not found at grain boundaries.

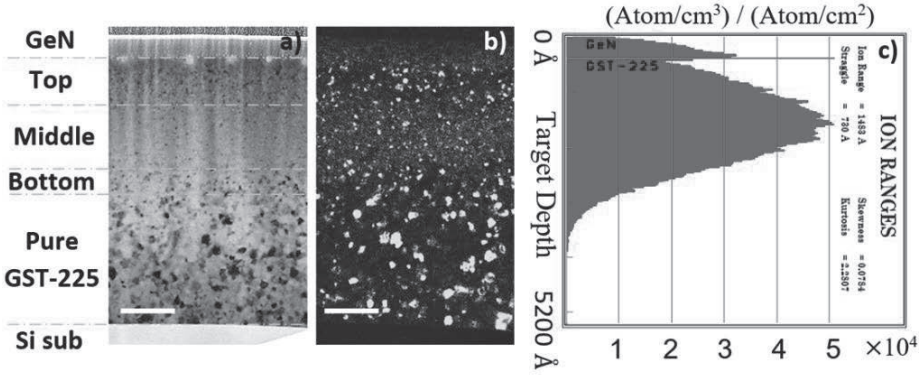

***Figure caption**: Bright Field (BF) TEM (a) and dark-field (DF) (b) images of the N-implanted GST-225 layer, annealed at 180 °C for 30 min. The N-implanted region is divided into different regions, the top, middle and bottom, which are N-implanted, and the unimplanted region which provides the pristine reference. (c) SRIM simulation of the N depth-distribution after implantation. The white bars show 100 nm.*

Keywords: phase change materials; implantation; in situ TEM; strain measurements, $Ge_2Sb_2Te_5$

Time Resolved Reflectometry with Pulsed Laser Melting of Implant Amorphized Si1-xGex Thin Films

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Nanosecond pulsed laser melting using a frequency doubled Nd:YAG laser (λ = 532 nm) was performed on implant amorphized Si and Si1-xGex thin films. Undoped pseudomorphic SixGe1-x thin films were grown to a thickness of 40 nm on (100) Si wafers and 10keV 1 x 1014/cm2 Ge+ implants were used to create a 15 nm surface amorphous layer. The dynamic evolution of the single pulse laser melt process was probed in detail by using in situ time resolved reflectometry (TRR) covering the sub-melt, partial melt (polycrystalline) and full amorphous melt (defective single crystal), to full epi-layer melt (defect free single crystal) regimes. TRR spectra were correlated as a function of energy density and Ge concentration with corresponding postirradiation cross sectional TEM micrographs. It was shown that the resolution of the amorphous to crystalline conversion based on reflectivity differences allowed for the distinction between solid phase and liquid phase epitaxy regimes. In fact, a full S curve description of the microstructural evolution was shown to be possible for the first time using TRR. Additionally, detection of the melt phase increased in sensitivity with increasing Ge concentration. Recovering the damage of implanted Si1-xGex is a crucial step in CMOS manufacturing, and the metastable microstructures produced by pulsed laser melting of Si1-xGex may be of interest for source/drain contact and channel strain engineering applications.

Optimization of Solid Phase Epitaxial Regrowth Assisted by UV Nanosecond Pulsed Laser

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3D sequential integration enables to stack several layers or devices on top of one another with a high contact density. However, its implementation faces the challenge of obtaining high performance top devices using a limited thermal budget. One of the main processes that must be adapted is the dopant activation in the source-drain regions. Currently, source-drain dopant activation can successfully be carried out through Solid Phase Epitaxial Regrowth (SPER) during a few minutes at temperatures as low as 450°C[1]. A nanosecond ultra-violet (UV) pulsed laser annealing is a promising option to further reduce the thermal budget[2]. In this work, we aim to optimize the SPER assisted by UV nanosecond pulsed laser in order to reduce the overall thermal budget and make it compatible with low temperature processes.

We report our results on the SPER of As implanted 70nm-thick SOI wafers. The arsenic ion implantation resulted in the amorphization of a 37-nm-thick layer as evidenced by cross-sectional Transmission Electron Microscopy (TEM) observations (Fig. 1 a)). The initial annealing strategy consisted in irradiating the sample with laser pulses at a constant energy density, 0.51 J/cm², close enough to the melting threshold to efficiently heat up the sample during each pulse and thus efficiently promote the SPER. Red squares in Fig. 2 illustrate the evolution of the sheet resistance, R□, as a function of the number of pulses, in comparison to a completely recrystallized sample (red dashed line). The R□ values of two additional samples ion-implanted with higher fluences are also plotted and show that this evolution is quite independent on the As fluence. The R□ saturation observed after irradiating with a large number of pulses indicates that, as the material recrystallizes, laser pulses become less effective and regrowth is slower and slower. We interpret that as resulting from the optical and thermal changes affecting the target as the thickness of the amorphous silicon layer decreases. To overcome this saturation, we implemented a new and different annealing strategy. Blue triangles in Fig. 2 show the R□ evolution corresponding to the process using the new strategy, with a saturation close to 200 ohm/sq for 500 pulses and above. Fig. 1 b) shows that a 25-nm-thick Si layer has recrystallized after 500 cumulative pulses. ToF-SIMS analysis showed that As did not redistribute during this laser annealing. The decrease of the thickness of the remaining amorphous layer during laser irradiation has been extracted from the data by calibrating the reflectivity using the time-resolved reflectometry values[2]. During each pulse lasting about 150ns, the maximum temperature was close to 800°C. The average recrystallization rate was close to 3e-4 nm/ns, a value 200 times faster than reported in previous works[3].

To sum up, we have studied in detail the recrystallization of As implanted amorphous Si thanks to irradiation with UV laser pulses. Taking into account the optical and thermal changes occurring as the thickness of the amorphous layer decreases, we have been able to propose a new strategy dramatically reducing the overall thermal budget received by the wafer. Further improvement will be possible by minimizing the total number of pulses needed to fully recrystallize the layers and activate the dopant. Latest results will be presented.

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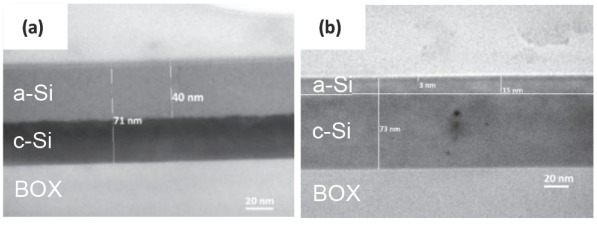

Fig. 1: Cross sectional TEM images of (a) an as-implanted sample and (b) a laser annealed sample with 500 cumulative pulses.

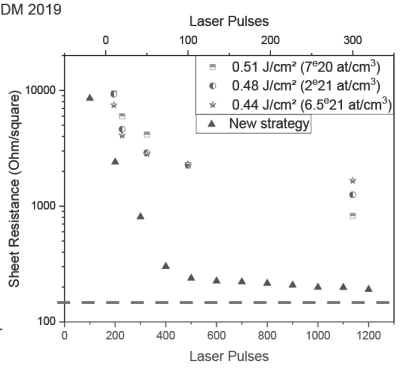

Fig. 2: Sheet resistance of three samples with different As concentrations after various number of pulses at different energy densities (half filled symbols), and with the new annealing strategy (blue triangles).

The red dashed line indicates the sheet resistance of a fully recrystallized sample in liquid phase for the lower concentration.

Continuum Simulations of the Evolution of Faulted and Perfect Dislocation Loops in Silicon during Post-implantation Annealing

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During post-implantation annealing, silicon self-interstitials (I) and silicon vacancies (V) generated during the implantation process are assumed to recombine, and the excess of Is are assumed to start to form clusters. For certain conditions, extended defects such as {311}-defects and dislocation loops, faulted (FDL) and perfect (PDL), are formed, as described by, e.g., Claverie *et al.* [1]. The dominating types of defects formed depend on the implantation damage as well as on the annealing temperature and duration. The damage evolution during annealing contributes to an enhanced dopant diffusion because of the resulting supersaturation of Is, and larger defects, when they form, may result in higher leakage currents in the final device. Computationally efficient simulation models, which describe the damage evolution, exist in the literature, for example [2, 3] to mention two. When it comes to the distinction between FDLs and PDLs, however, further calibration is needed to better capture their evolution during annealing. A new calibration, based on experiments reported in the literature, is the focus of this work.

Dislocation loops are typically associated with higher implantation doses and higher thermal budgets, used in the manufacturing of, e.g., power electronic devices and solar cells. The model from Zographos *et al.* [2] includes small I-clusters up to a certain size, and uses moment-based approaches to describe {311}-defects and dislocation loops. The model is already available in Sentaurus Process of Synopsys, but it does not distinguish between FDLs and PDLs. Wolf *et al.* [3] found that the model in [2] resulted in too high dissolution velocities of loops at high temperatures. To account for that, the model in [2] was extended to include PDLs as well [3]. Wolf *et al.* [3] also modified the model for the loop radius to include I-exchange among extended defects (conservative), and between extended defects and other sources and sinks (non-conservative). Nonetheless, for the calibration, the focus of Wolf *et al.* [3] was still on the sum of dislocation loops, and not so much on the distinction between the two types.

In this work, the focus was to recalibrate the model in [3] to better describe measured data of PDLs and FDLs after post-implantation annealing. The better the individual defect types can be described, the clearer will the overall picture be, contributing to better predictions of enhanced dopant diffusion as well as of performance deterioration due to leakage currents in the final device. The calibration in this work is still ongoing, but an intermediate result is shown in Fig. 1. It shows experimental data of end-of-range defects from Cristiano *et al.* [4] of Ge implanted silicon (2×10^{15} cm^{-2}, 150 keV) followed by rapid thermal annealing (10 - 400 s) at 900 °C (N_2 ambient), together with the corresponding simulation results using the latest calibrated parameters and the parameters from [3]. Already the latest results of the calibration better capture the trends of the data, indicating more and larger FDLs forming than PDLs in agreement with the experiments and in contrast to the original model calibration. However, there is still room for improvement, especially for the mean loop area of PDLs. The calibration is not yet finalized and Fig. 1 will be updated for the full paper, which also will contain additional experiments from literature not shown here (e.g., from [4] and [5]), together with corresponding simulation results.

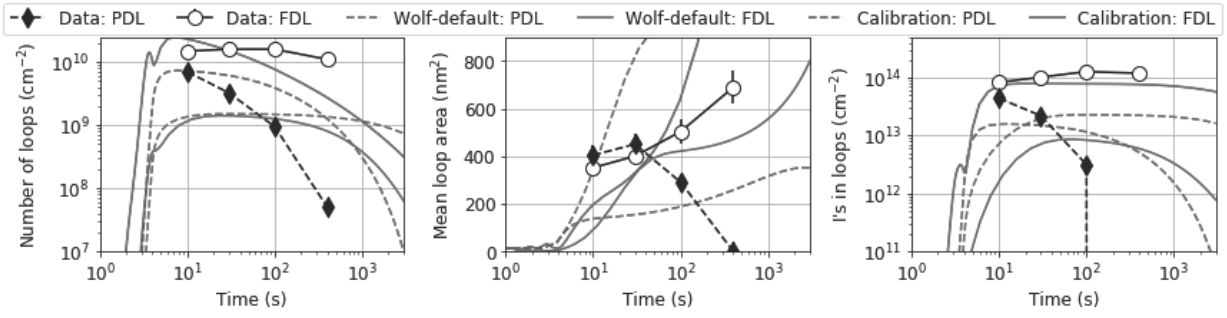

Figure 1: Evolution of faulted and perfect dislocation loops during RTA at 900 °C in N_2 ambient after implantation of Ge into silicon (2×10^{15} cm^{-2}, 150 keV). Measured data from [4] and simulation results using the model in [3] with default and calibrated parameters.

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Integration Technologies for *pn*-Stacked TMDC CMOS Devices

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Device applications are discussed especially on the doping and annealing processes in 2D semiconductor materials, such as transition metal di-chalcogenide (TMDC) film, for future LSIs.

In order to improve the performance of integrated circuits, it is necessary to control the semiconductor channel thinner than 5 nm in the FinFET and gate-all-around (GAA) nano-sheet (NS) FETs [1–8]. However, electron- and hole-mobility values are seriously reduced in silicon, germanium and other 3D-crystal semiconductors [11]. In addition, in order to improve the density of transistors per chip area, pn-stacked CMOS devices (so-called CFET) is required to be achieved [9, 10]. Therefore, the transition metal di-chalcogenide (TMDC) film with higher mobility rather than silicon and germanium in the thickness less than 3 nm is aggressively investigated [12–14], hopefully in the stacked TMDC films, as shown in Fig. 1. As the integration technologies for the pn-stacked TMDC CMOS devices, a sulfur-vapor annealing for MoS_2, WS_2 and ZrS_2 films effectively improves their crystal qualities, resulting in the normally-off *n*MISFET with an accumulation operation with the low-carrier-density MoS_2 channel [15–26]. To further enhance the device performance, doping technologies are needed to be achieved hopefully with self-aligned method even for the pn-stacked TMDC CMOS devices [27–32].

Based on such various integration technologies, the pn-stacked TMDC CMOS devices are strongly expected to be achieved for a greener society.

Acknowledgements

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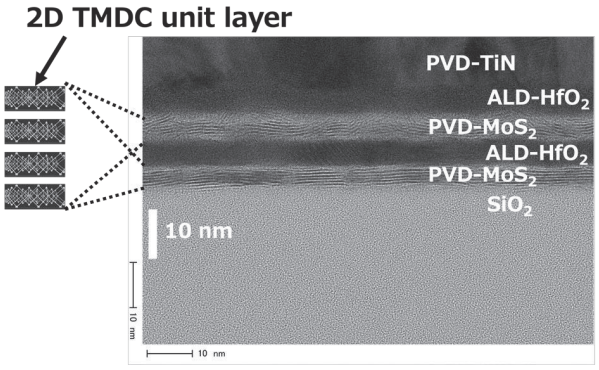

Figure 1: Stacked PVD-MoS_2 films sandwiching ALD-HfO_2 film and capped with PVD-TiN film hopefully for pn-stacked TMDC CMOS devices.

The Performance of the Fourth Generation of Safe Delivery Source® (SDS®4) Package on AIBT iPulsar High Current Implanter

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Abstract. The dopants used in ion implantation often pose a safety risk due to their inherent hazards, and these risks need to be considered when selecting the material delivery system. Entegris has developed the SDS® product family that minimizes risk by adsorbing the gas in a non-compressed state. SDS4 is the fourth generation of the safe delivery source (SDS) which is the leading packaging solution for subatmospheric specialty gas storage and delivery for ion implanters. In this paper, we present results of performance tests for SDS4 Phosphine (PH_3) and Arsine (AsH_3) gases on a 300mm AIBT iPulsar high current implant tool. The performance is compared to the current process of record (POR) which is the delivery of these gases in SDS3 cylinders. The beam performance, beam spectra, implanted test wafers, doping profile and contamination results are evaluated.

Keywords. SDS, SDS4, safe delivery source, implant, phosphine, PH_3, arsine, AsH_3

Investigation of Various Source Materials and Co-gases for Fluorine Ion Implantation Performance Improvement

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Abstract. In advanced semiconductor device manufacturing, fluorine implant is commonly used to enhance the shallow junction formation and improve the electrical characteristics of the transistors. Typically, this implant is done using common fluorine containing dopant gases, such as BF_3, GeF_4 or SiF_4. The F^+ beam performance of those materials was tested and reported previously. [1] In this paper, additional dopant feed gases, and mixtures are tested with the purpose of further improving the F^+ implant beam performance. The results of this study identify optimized conditions for improving the F^+ beam current and increasing the ion source lifetime for this application.

Keywords. Fluorine implant, fluoride gas, dopant gas, ion implantation, beam current

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Germanium Ion Implantation Performance Improvement on Applied Materials' VIISta HCS High Current Implanter with Use of Germanium Tetrafluoride (GeF_4) and Hydrogen (H_2) Mixture Gases

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Abstract. Germanium Implant is a key materials modification implant step that is used in semiconductor wafer manufacturing. In this implantation process, germanium tetrafluoride (GeF_4) is commonly used as the primary feed gas. The use of a fluoride-based gas, such as GeF_4, often leads to poor beam and source life performance due to the effect of the halogen cycle. In this paper we present data which highlights a performance improvement when using EnrichedPlus $^{72}GeF_4$ and hydrogen (H_2) mixture as an alternative to enriched $^{72}GeF_4$. The benefits of the mixture gas include both an increase in beam current as well as longer ion source life which allows for greater tool productivity. These results were achieved on an Applied Materials' VIISta HCS high current implanter that was running in a high-volume manufacturing environment.

Keywords. ion implant, VIISta, dopant, germanium, germanium tetrafluoride, GeF_4, enriched, hydrogen, H_2, mixture, productivity, beam current, source life

Performance Improvement on SMIT SHX-III High Current Ion Implanter through the use of EnrichedPlus ^{72}Germanium Tetrafluoride (enPLUS $^{72}GeF_4$) and Hydrogen (H_2) Mixture Gases

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Abstract. Implantation of Ge^+ ions is a critical materials modification implant used in the manufacture of semiconductor devices. When performing this implant, the production tool often suffers from low productivity due to the halogen cycle and tungsten deposits which limit the ion source lifetime. This paper explores the performance improvements achieved on a SMIT SHX-III high current ion implant tool by using a mixture of EnrichedPlus $^{72}GeF_4$ and H_2 versus the standard process of natural GeF_4 only. Data are presented showing a beam current improvement of approximately 2x, and an increase in ion source life of more than 6-fold. In conjunction with the material change to EnrichedPlus $^{72}GeF_4/H_2$ mixture, this paper also discusses optimized procedures that were implemented which contributed to the significant increase in tool productivity.

Keywords. ion implant, dopant, germanium, germanium tetrafluoride, GeF_4, enriched, hydrogen, H_2, mixture, productivity, beam current, source life

Investigation of Source Materials, Co-gases, and Methods for Aluminum Ion Implantation

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Abstract. Silicon carbide is one of the major semiconductor materials used for manufacturing innovative power devices, especially for high power applications. Aluminum is the primary implant species that is used for p-type doping of silicon carbide (SiC) power transistors. Because there are no suitable aluminum gaseous dopant sources available for ion implant, the most common approach is to generate aluminum ions by installing a solid aluminum target inside the arc chamber. The solid target is then reacted, through physical and chemical mechanisms, by using argon and/or a fluoride containing gas. Presented here, we examine both aluminum oxide (Al_2O_3) and aluminum nitride (AlN) targets in combination with different co-gases to assess Al^+ implantation performance. The gases tested include boron trifluoride (BF_3), phosphorus trifluoride (PF_3) as well as other fluoride gases and their mixtures. The performance factors characterized include aluminum beam current, beam spectra, and source conditions for each of the various options. This work concludes with a recommendation on the optimal solution for the aluminum implant application.

Keywords. power device, silicon carbide, SiC, aluminum, implant, aluminum oxide, Al_2O_3, aluminum nitride, AlN, boron trifluoride, BF_3, phosphorus trifluoride, PF_3

Performance and Reliability of the Fourth Generation of Safe Delivery Source® (SDS®4) in the Ion Implantation Application

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Abstract. Safety and reliability are important considerations for the ion implantation process, which uses hazardous gases to make semiconductor devices. Entegris' Safe Delivery Source (SDS®) adsorbs these gases onto porous carbon for subatmospheric storage and delivery. The immobilization of the gas in the adsorbent dramatically reduces the release rate potential versus a comparable high-pressure cylinder. Since its' inception, the adsorbent used in this subatmospheric gas storage and delivery system (Type 1 SAGS) has been continuously optimized based on evolving customer requirements. The next generation of Type 1 SAGS technology, SDS4, strives not only to solve the difficulties of the ever-increasing demands of the semiconductor industry but also proactively address future challenges.

In this paper, we will present performance and reliability data to support the positioning of SDS4 as the premier choice for the delivery of ion implant dopants. The discussion includes both the cylinder package design as well as the functional testing that validates the performance and reliability of the product in the application. The cylinder design features that are presented include an improved particle filter, new cylinder valve, gas purity and an increase in gas deliverable capacity. All these features are validated for performance through testing on an ion implant tool. In addition, the long-term reliability of the product was confirmed through functional testing which validates performance over entire product lifecycle. The combination of a tested design that leverages the foundation of previous versions of the SDS product line, along with confirmation testing in the application, proves that SDS4 provides the features that are necessary to meet the requirements of the semiconductor industry.

Keywords: SDS, SDS4, Safe Delivery Source, Gas Adsorption, Specialty Gases, Ion Implantation

Charge Transport in Doped and Strongly Coupled Nanocrystal Films

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Abstract

Inorganic colloidal nanocrystals (NCs) are of great interest in solution-processed electronic and optoelectronic devices such as field-effect transistors (FETs) solar cells, light-emitting diodes (LEDs), and lasers. However, charge transport in NC film is seriously hindered by weak interparticle coupling as well as surface depletion regions resulting from the presence of surface states. Recently, the advent of engineering surface ligands for enhanced electronic coupling and surface trap state passivation through surface doping resulted in high-mobility charge transport in NC films, making these build blocks promising for a variety of applications. A combination of optical, chemical, and structural properties and temperature-dependent electrical conductance demonstrates that post-synthetic process developed in our studies successfully modifies the surface chemistry of the NC films for charge transport. In this study, we will discuss 1) how surface chemistry and doping can enhance electronic transport in semiconducting NC solids and 2) how different types of NCs can be utilized as promising components for the low-cost, large-area fabrication of nanocrystal device technologies.

Keywords: Thin film, electronic material, surface chemistry, electrical properties

Results and Adoption of Safe Delivery Source® (SDS®4) on VIISta® HCP

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Abstract. Semiconductor device requirements continue to focus on dopant material quality as device technology expands in advanced automation, especially safety sensors and processing of collision avoidance signals. These requirements cause end users to focus on quality for all of their processes including dopant materials. SDS®4 addresses these requirements by expanding on the sub-atmospheric gas source type 1 (SAGS1) cylinder package of SDS3. SDS4 includes an updated cylinder valve design, an improved internal manufacturing process and a more comprehensive quality data package. This enables implant and device engineers the most accurate dopant quality data in the SAGS 1 market. This paper compares SDS4 to SDS3 performance criteria in a manufacturing environment, and validates that the SDS4 package maintains all safety characteristics, while increasing gas deliverables, employing a better valve design, and offering superior product data.

Keywords. SDS, SDS4, SDS3, safe delivery source, implant, phosphine, PH_3, arsine, AsH_3

How Safe Is a Safe Dopant Gas Delivery System?

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Dopant gases used in ion implantation are poisonous and flammable (hydrides) and toxic and corrosive (fluorides). In the last 20 years, safe dopant gas delivery systems were developed to reduce the risks associated with handling and using dopant sources in ion implanters. Two types of technologies are currently in use to achieve these safety and environmental improvements: nano-porous materials to adsorb the dopant gases (Type I) and the use of in-cylinder mechanical devices to lower the delivery pressure from high-pressure vessels (Type II). Both technologies provide substantial safety advancements compared to conventional high-pressure cylinders albeit type I systems are recognized as intrinsically safe as the dopant gases are stored at sub-atmospheric pressures. This feature is a major safety advantage as an accidental valve opening of a high-pressure vessel would result in a rapid and catastrophic gas release that could harm humans and the environment. To date, two type I products are commercially available differentiated by the type of adsorbent being used: activated carbon (beaded or monolithic shaped) or metal organic frameworks (MOFs), a new class of high-surface area materials used in ION-X. One area of safety concern is the impact of accidentally opening or forgetting to close a type I cylinder valve after use: As opposed to high pressure gas releases, this event results in air rushing into the cylinder reacting with the stored dopant gas and adsorbent. In this paper, the effects of opening a full (1 Kg arsine at 650 Torr) and nearly empty (20 Torr of pressure) ION-X cylinders to air will be reported. The results are compared to published arsine release tests using carbon-based products where full cylinder release tests resulted in measurable quantities of arsine leaking out moments after opening the cylinders. Using similar conditions and timed events, the release test experiments using full and nearly empty ION-X cylinders resulted in non-measurable levels of arsine released from the cylinder. In addition to the experimental details and results, this article hypothesizes on the fundamental physical and chemical differences between carbon and MOF adsorbents responsible for the different outcomes.

Dopant Gas Purity and Adsorbent Stability

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Dopant gases used in ion implantation are poisonous and flammable (hydrides) and toxic and corrosive (fluorides). In the last 20 years, safe dopant gas delivery systems were developed to reduce the risks associated with handling and using dopant sources in ion implanters. Adsorbent-based gas sources comprise of gas cylinders filled with high surface area nanomaterials that reversibly adsorb dopant gases inside their pores. These cylinders are considered intrinsically safe as the dopant gases are stored at sub-atmospheric pressures. To date, two adsorbent-based dopant gas delivery systems are commercially available differentiated by the type of adsorbent being used. SDS2 and SDS3 cylinders use activated carbon while ION-X use metal organic framework (MOFs). Metal-Organic Frameworks (MOFs) are a new class of nano-porous materials comprised of organic ligands and metal nodes creating highly uniform crystalline structures. By changing the ligand and metal units used to build MOFs, tens of thousands of structures can be created with custom surface areas, pore sizes, and reactivities. The MOFs used in ION-X were specifically designed and extensively tested for their dopant gas compatibility, stability, and delivery performance. Gas quality delivered from adsorbed systems are related to the absorbent purity, pore size distribution, and absorbent/absorbate reactivity. In this article the stability of MOFs used in ION-X will be characterized and contrasted to activated carbon. In addition, the gas purity extracted from MOF adsorbents will be compared to high pressure and competitive products to further demonstrate the superior stability and durability of the adsorbents.

Temperature Effect in High Dose, Medium Energy Implantation with Single-Wafer-Type Implanter

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In power device fabrication, the high dose implantation at medium energy range has been performed with traditional high-current implanter of batch type. While the power device production rapidly has been shifted to the 300mm line, it is necessary to beware of two factors which increase the crystal damage [1]. The one factor is a transition to the single-wafer-type implanter to eliminate the angle deviation. The other factor is an increase of the beam current (I_b) for compensating the throughput, which is reduced due to the larger wafer size.

In this study, the characteristics of the high dose BF_2 implantation were investigated considering the crystal damage with the SMIT's single-wafer-type implanter, SAion. For BF_2 70keV 2×10^{15} ions/cm^2, as increased the I_b, the sheet resistance (Rs) was also increased as shown in Fig.1. This could be attributed to the degradation of carrier concentration and/or mobility due to the crystal damage caused by high I_b. Wafer temperature during implantation is considered a key factor for controlling Rs as wafer temperature is an effective parameter for changing the crystal damage, so that, the dopant profiles were matched between different type of implanters in the previous work [2]. As a result, by increasing the wafer temperature, the Rs difference between I_b=1mA and I_b=4mA was dramatically reduced. For the better understanding about the crystal damage and the dopant behavior, XTEM, SIMS and SRA analyses were also performed.

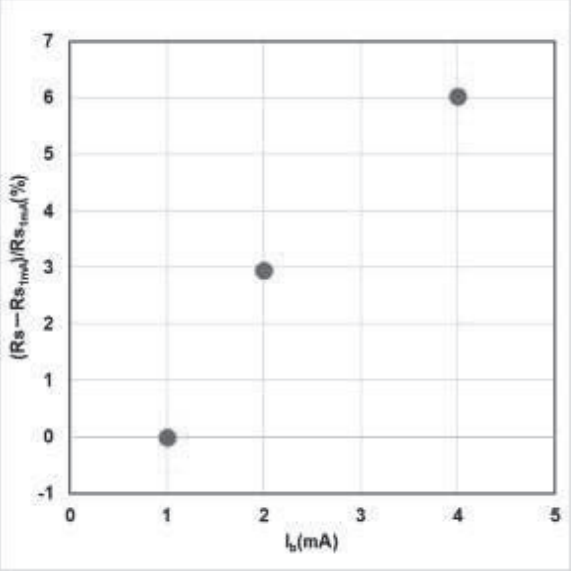

Figure1. Variation I_b and Rs

[1] G. Fuse et al. IIT2004, pp. 77-82
[2] T.H. Huh et al. IIT2008, pp. 87-90

Ionization Induced Carbon Phase Changes in Graphite

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We have studied changes in highly-oriented pyrolytic graphite (HOPG) after MeV ion bombardment in order to assess the effect of ionization on the atomic bonding of carbon in the material, using X-ray photoelectron spectroscopy (XPS), Raman spectroscopy, and 3D laser microscopy. We also observed the hexagonal carbon ring structure of graphene sheets in graphite using AFM in order to assess any changes in carbon bond length or distortion of the hexagonal lattice due to the passage of ionizing particles. Rutherford backscattering spectrometry (RBS) and x-ray photoelectron spectroscopy (XPS) were used to identify impurities in the material and their potential impact on graphite surface properties. RBS was used because most impurities are significantly heavier than carbon, and therefore they can be easily detected and quantified without any need for substrate background subtraction. XPS was used to confirm the RBS findings and identify any differences in the distribution of impurities in the bulk and at the surface of the material before and after MeV implantation.

Changes in the material bonding was quantified using x-ray induced AES (XAES) and Raman spectroscopy to measure the fraction of graphitic sp2 and diamondlike sp3 phases before and after MeV implantation. The general trend of conversion of sp2 bonded carbon to sp3 phases was confirmed with increases in ionization density, as well as some significant surface disruption observed by 3D laser microscopy, may be explained by rapid thermal quenching following MeV ion-induced excitation.

Oral or Poster: Oral
Proposed sessions: Implant/Doping Technologies and Processes

Enhancement of Al^+ Beam Current in GSD III-180

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In recent years, the demand for SiC semiconductor has been rapidly increasing in fields such as power saving equipment. Aluminum (Al) is a p-type dopant in SiC and has been implanted at dose of wide range in SiC device fabrication. In production, it is necessary to effectively generate Al^+ at an ion-source in order to obtain high beam current in ion implanter. In the typical method of utilizing a vaporizer, Al^+ beam currents of ~10^1 μA for solid Al material and ~10^2 μA for aluminum fluoride (AlF_3) can be obtained. However both are insufficient for production.

In this study, we focused on source material and carrier gas at the ion-source in order to enhance Al^+ beam current. In the GSD III-180; Sumitomo Heavy Industries Ion Technology's high-current batch type implanter, some trials were performed to improve amount of Al^+ generation. First, AlF_3 powder and Al grains were uniformly filled inside a vaporizer as a source material and were combined with Ar carrier gas which flows into arc chamber. Figure 1 shows the dependence of beam current in a 60 keV Al^+ on Ar gas flow rate under the mixed material. The beam current shows maximum value at gas flow rate of 1.5 sccm. This results from competition between generation and disappearance for Al^+. Next, Ar was replaced by BF_3 as the carrier gas. The flow rate dependence is shown in the same figure. The beam currents with BF_3 is significantly increased compared to those in Ar. The cause is considered to be that fluorine from BF_3 and AlF_3 chemically erodes Al in the source plasma and contributes to gasification of Al. By optimization for other parameters such as temperature in vaporizer, an Al^+ beam current of up to 5.3 mA can be obtained with a source material mixture of 1:1 with BF_3 carrier gas.

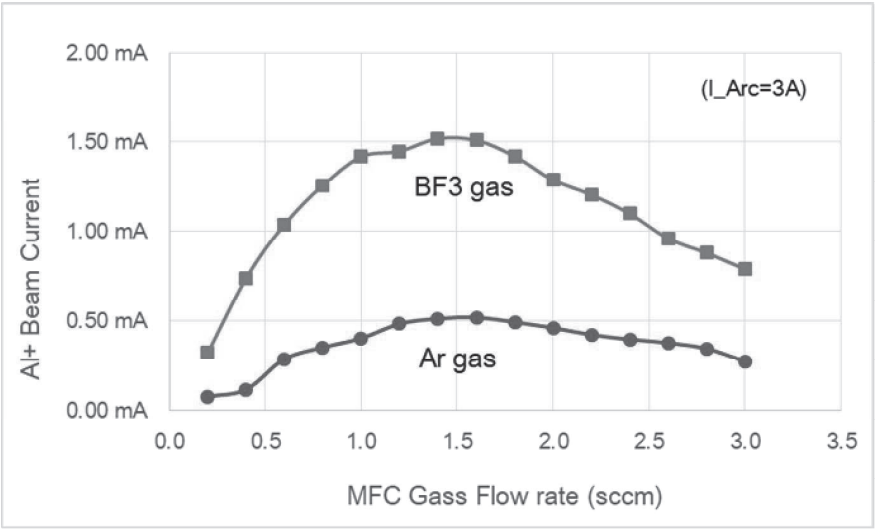

Figure1. The dependence of beam current on gas flow rate in Ar and BF_3 with an equal mix of Al and AlF_3 source materials.

A Study of Beam Divergence Effects for Medium Dose Channeling Implants

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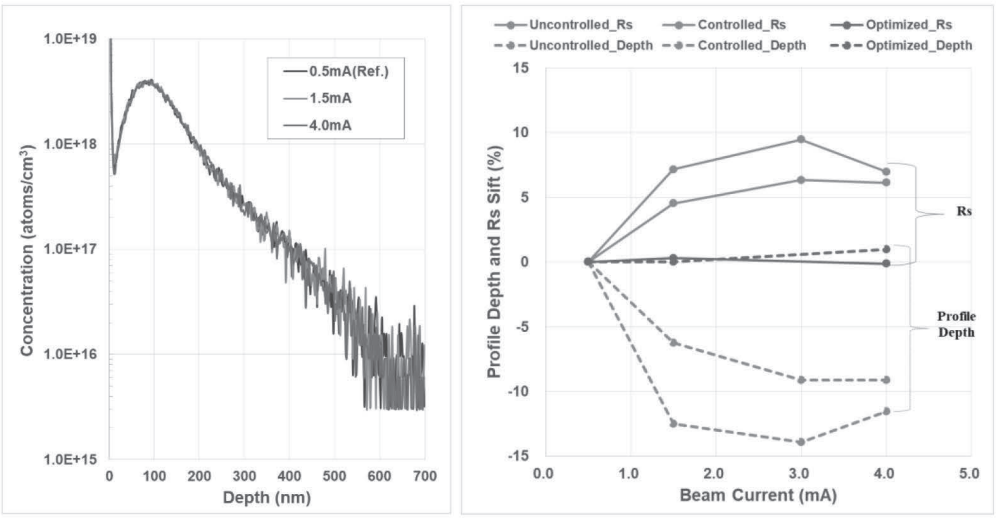
Accurate beam angle control has become increasingly important as IC device sizes have scaled down and with the wide use of 3D vertical structures. Especially for the channeling (0 degree tilt angle) implants, both beam steering and divergence angle should be carefully controlled to get the desired dopant profile. In this paper, beam divergence effect on channeling implants was investigated with SMIT's new divergence angle control and monitoring system for the SAion implanter [1]. The divergence angle was controlled with SMIT's new beam control system, triplet quadruple and Einzel lens, and monitored with the On-Plane beam steering and divergence measurement system. For medium dose channeling conditions, for 50 keV $^{31}P^{+}$ beams, the junction depth became shallower and the sheet resistance (Rs) became higher with increasing beam current because of the Self Channeling Reduction Effect of higher beam current. To overcome this effect, that is, to get same dopant profile depth, it was necessary to control the beam divergence very carefully. In this study, three type of the beam divergence control modes were used; Uncontrolled (larger divergence for higher beam currents), Controlled (same divergence for all beam currents) and Optimized (smaller divergence for the higher beam currents). For the Optimized mode, by suppressing the beam divergence for the higher beam current, the depth profile [Fig. 1(a)] and sheet resistance [Fig.1(b)] were nearly unchanged over an 8x range of beam currents. In addition, the species dependency was also investigated.



(a) (b)

Fig.1. (a) The beam current dependency of the SIMS profile at the optimized beam divergence. (b) The beam current dependency of the sheet resistance (Rs) and the profile depth at 5E17 atoms/cm^3 for the various divergence control modes.

Reference

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Ion erosion and particle release in fine graphite

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Given the general interest in ion erosion of graphite in the degradation of beamline components and as a source of particles, direct data in graphite erosion rates and particle release under conditions of interest for commercial ion implantation operations is remarkably sparse in the public literature. Accordingly, a program of ion erosion and particle studies was begun and initial results reported at IIT18 [1]. This study reports results from 12 graphite types with a variety of surface treatments. Samples were exposed to a 6 mA, 40 keV Ar+ beam in the flag Faraday location of an NV-10 beamline for ≈10 hours, for an accumulated dose of ≈3e19 Ar/cm^2. Ion erosion depths were measured by optical scanning and particles released by a tape lift-off were imaged with optical and SEM tools at Covalent Metrologies, Sunnyvale, CA. Systematic effects were seen in erosion depths with selected bulk properties. SEM imaging revealed contrasting surface topologies for particles released from graphite with various surface treatments. Trends related to graphite bulk properties will be discussed.

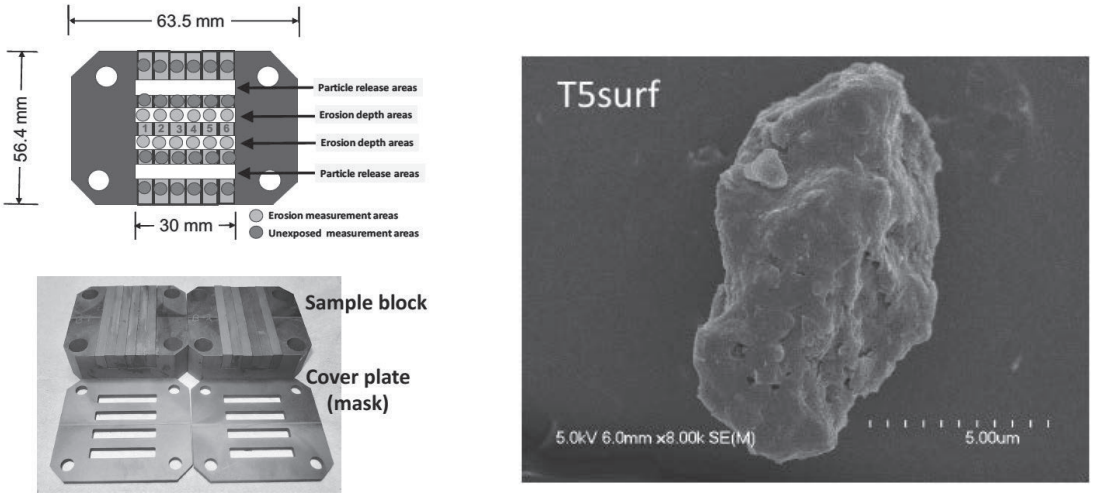

Figure 1. Layout of graphite samples, ion mask and holder with photo of two loaded sample sets ready for implant (left) and example SEM of a particle released from an implanted graphite surface with a specailized surface treatment (right).

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Profiles and defects in highly-channeled and random beam orientation MeV dopant implants in Si(100)

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Low-dose 7.5 MeV B and 10 MeV P and As profiles in Si(100) with "random" (7/23 tilt/twist angles) and highly-channeled (0/0) beam-crystal orientations were studied with SIMS and the MC-code, IMSIL, profiles and a variety of carrier recombination sensitive defect metrologies. These studies were extensions of earlier papers presented at IIT18 [1] and IWJT19 [2]. As-implanted and annealed (950 C/ 3 min/ N_2) samples were characterized by: (1) Photoluminescence (PL) imaging and spectral power levels. Systematic effects of defect-related PL data are related to beam incidence along highly-channeled and "random" beam-crystal orientations. Time signatures of curious "intermittencies" in the PL signals will also be discussed.

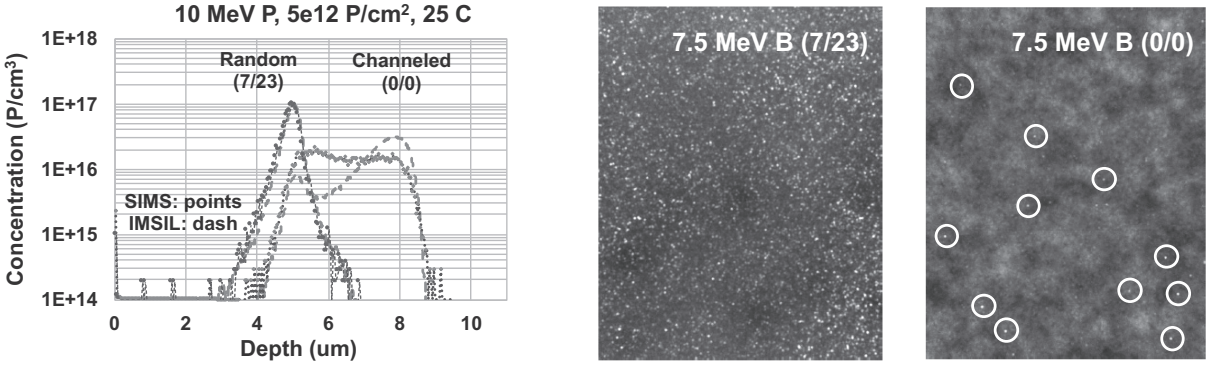

Figure 1. SIMS & IMSIL profiles for random and channeled 10 MeV P implants at a dose of 5e12 P/cm^2 (left) and PL images for random and channeled 7.5 MeV B implants at a dose of 3e12 B/cm^2 (right). Note the dense recombination centers in the random PL data for 7.5 MeV B.

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PL and SRP Studies of Phos Implants

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A diverse set of 22 different Phosphorous implants into Si(100) over a dose range from 3e13 to 3e14 P/cm^2 and at energies of 10 keV to 1 MeV were studied with Photoluminescence (PL) and Spreading Resistance Profile (SRP) methods. In addition to single Phos implants, mixed species and energy Phos with Carbon implants were also studied. Anneal conditions at 850 and 1000 C were compared. SRP data were compared with SIMS and Monte Carlo IMSIL profiles. Correlations between implant conditions and measured effects and implications for process control applications will be discussed.

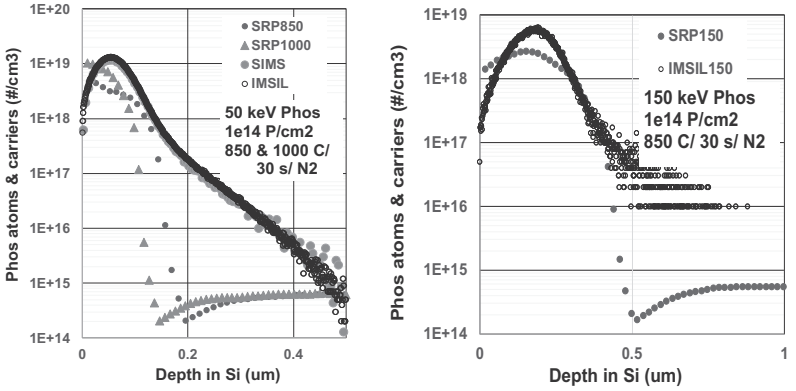

Figure 1. SRP, SIMS and IMSIL profile for 50 and 150 keV Phos implants annealed at 850 and 1000 C showing incomplete dopant activation for lower energy profiles.

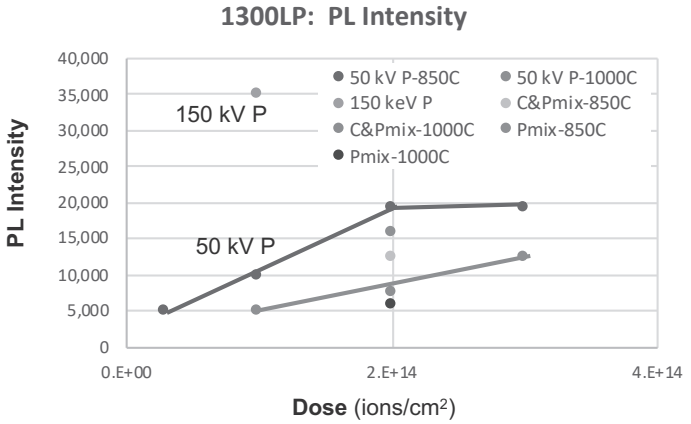

Figure 2. PL intensity data for 50 and 150 keV Phos implants annealed at 850 and 1000 C, showing lower defect-delated PL intensity for higher temperature anneals for single ion and mixed species (P & C) implants. The "Pmix" doping is a combination of 50 and 10 keV P^+ implants, simulating a n-source/drain contact, with and without a 10 keV C co-implant.

Ion erosion and elemental purity of deposited Si films on Al

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Deposited Si films are often used to reduce metal contamination for beam line and wafer fixturing components exposed to ion beams in implantation equipment. The erosion-limited lifetime of these Si films depends on the density, adhesion and thickness the deposited Si films. In this study, direct measurements of the erosion rates, surface texture, density and metal contamination levels were made for plasma spay, CVD and PVD-deposited Si-on-Al strips and crystalline Si. Samples were mounted in a modified graphite holder design used in other studies of ion erosion [1], placed in the flag Faraday location of an NV-10 beam line and exposed to 40 keV As^+ beams, accumulating doses between 7e17 to 4e19 As/cm^2. Additional samples were exposed to 30 keV Ga^+ beams in a FIB system. Erosion depths were measured by several optical profilometry methods, surface texture was inspected with SEM and RBS was used to measure Si density and heavy metal contamination levels. Spray-Si films were less dense and eroded up to 30% deeper depths than PVD and CVD films and c-Si. Significant Fe was observed in the plasma-spray materials. Erosion data and nuclear stopping powers were used to estimate the sputter-limited lifetimes of deposited Si films exposed to high doses with common dopant ion beams at various energies.

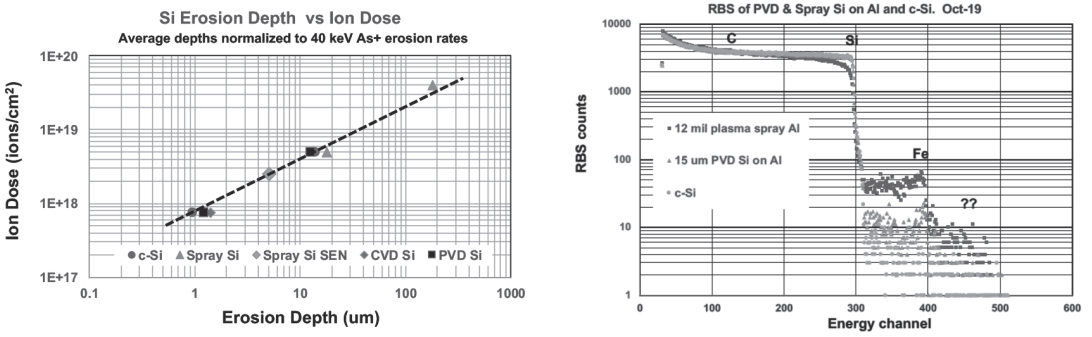

Figure 1. Si erosion depths vs. dose of various Si materials for 40 keV As^+ beams (left) and RBS data for plasma spray and PVD-deposited and c-Si, showing lower surface density and higher Fe contamination in the plasma spray-Si film (right).

[1] M.I. Current, T. Ido, Y. Horio, H. Fujibuchi,"Ion Erosion and Particle Release in Graphite Materials", IIT18 (2018).

Individual Dopant Profiles in High Energy Multiple Implantation under Channeling Conditions

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The multiple implantation steps at high energy are essential for formation of deep and smooth dopant profiles in the photodiode region of CMOS image sensors. A series of implantations is performed with tilt angles nearly equal to 0° from the Si(100) axial direction to intentionally obtain direct channeling conditions. Damage in Si substrates from the stopping of ions during the multiple implantations depends on ion type and implantation energies and increases with the accumulated dose. After the initial implantation step, the channeling conditions are influenced by the accumulated damage from the earlier implantations. In this paper, we examine the effect of damaged Si substrates on individual dopant profiles in multiple channeled implantation steps. Figure 1 shows SIMS profiles for As multiple implantations, at energies from 1 MeV to 5 MeV, with the higher energies implanted first. In profile (a), As implantations range from 2 to 5 MeV in 1 MeV pitch. In profile (b), a 1 MeV As step is added to the 2 to 5 MeV sequence. The effect of the 1 MeV As implantation can be seen in the first 3 μm of the combined profiles. The difference in the combined SIMS profiles, (b-a), has a peak that is significantly shallower with a steeper tail than a single 1 MeV As profile into undamaged Si, showing the effects of the combined damage in the earlier, higher energy As implant steps. To estimate the effect of prior implantation damage on channeled As profiles, the 2 to 5 MeV sequence was replaced by a P multiple implantation. Figure 2 shows SIMS profiles of channeled 1 MeV As profiles into undamaged Si(100) and after multiple implant sequences with P ions at energies of 1 to 5 MeV, in 1 MeV pitch and individual doses of 3×10^{12} P/cm^2, implanted under channeled (0°/0°) and random (7°/23°) beam orientations. The channeled tail seen in the 1 MeV As profile into undamaged Si(100) is reduced by the damage from the prior multi-step P implantations, with the shallower and higher levels of damage from multiple P implantations under random beam orientation (non-channeled) conditions having the largest effect. It can be seen that the damage caused during multiple implantation reduces the degree of channeling in subsequent implantations. Multiple channeled implantation sequences are also modeled with IMSIL MC calculations.

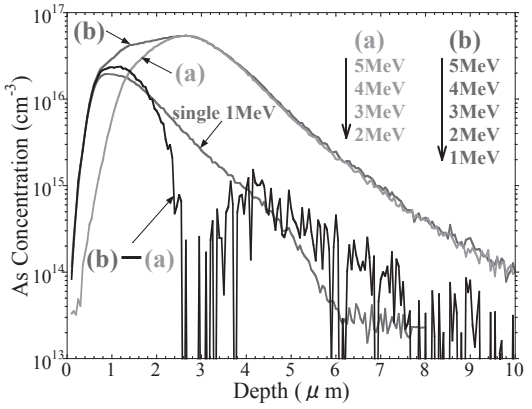

Fig.1. SIMS profiles for channeled As multiple implantations and a single 1 MeV As. Profile (a) is from a multiple As implantation at 2, 3, 4, and 5 MeV, each step at 3×10^{12} As/cm^2. Profile (b) is a channeled multiple As implantation that includes energies from 1 to 5 MeV.

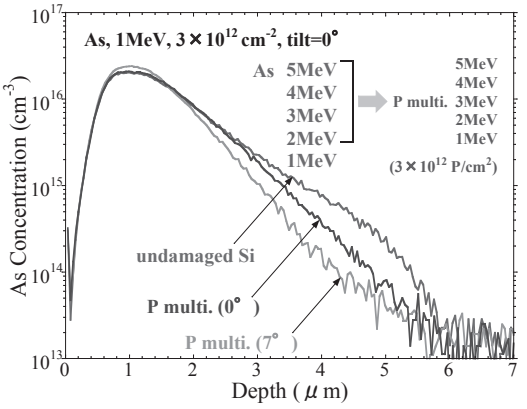

Fig.2. SIMS profiles for channeled 1 MeV As implantations into various of Si substrates; undamaged Si(100) and Si with prior multiple implantations of 1 to 5 MeV P with channeled and random beam orientations.

Beam shape control system by machine-learning on the NISSIN BeyEX medium current ion implanter

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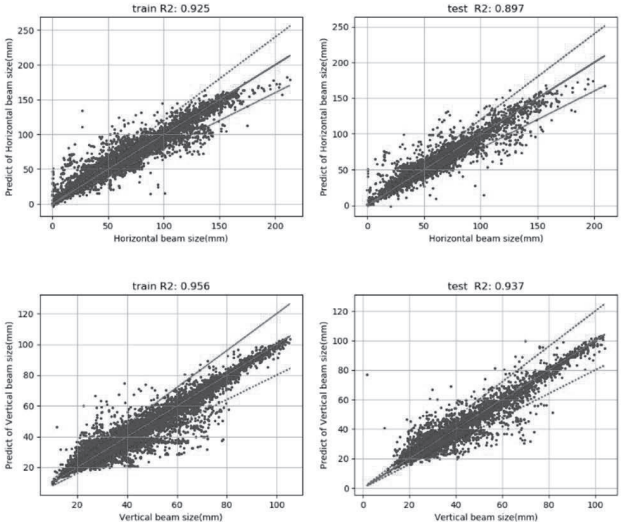
In the ion implantation process for semiconductor device fabrication, beam shape is one of the most important physical quantities affecting device characteristics. However, controlling the beam shape requires accurate monitoring of the beam shape and complex adjustment of multiple beam tuning parameters according to the ion implantation conditions, which is difficult to automate by rule-based programming.

In this study, we developed and evaluated an automatic parameter tuning system that uses machine learning to infer and output optimal parameters based on the current beam condition and equipment condition as training data.
The system sets the target beam size for arbitrary beam conditions (ion species, energy, and beam current) in advance, and performs beam setup within the range of the target beam size.

The following figure shows the results of the system training. The system obtained a coefficient of determination of more than 90% for train data with the target beam size in vertical and horizontal directions.



Scaled FinFET Well Formation Using Heated Implantation

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FinFET doping via implantation at room temperature could result in Fin damage within the Fin body and degrade Fin device performance. Heated implantation techniques are developed on Thermion® VIISta platform implanters to address the detrimental effects on devices caused by the damage, such as LDD formation [1, 2].

For well formation, there are two implant-based approaches: 1) using implant through Fin scheme, the implant damage can result in Fin damage especially for scaled Fin technology with elevated well implant dose required to suppress sub-fin leakage; 2) using the implant/epi scheme, the residual damage before epi process could result in Fin crystal defects and therefore be detrimental to device performance. In this paper, the heated implantation technique was applied to typical well formation conditions. Post heated implant wafers were characterized with TW damage, Rs for activation, and SIMS for profile response at various implant temperatures for boron (B), phosphorus (P), and arsenic (As). TCAD simulations are explored to understand the Fin well requirement to suppress sub-Fin leakage with evolved Fin technologies. For implant/Epi scheme, TCAD simulations predict the damage control required for multiple well/punch through implants. Experimental studies showed damage free epi growth with elevated implant temperatures.

1. L.C. Pipes, et al., “NMOS Source-Drain Extension Ion Implantation into Heated Substrates,” IIT 2014, pp. 37-42.
2. T.Y. Wen, et al., “FinFET IO Device Performance Gain with Heated Implantation,” IIT 2018 pp. 106-109.

Analysis of Dopant Distribution Profiles of Very High Energy Implants

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Technology advances in products such as CMOS image sensors, discrete power devices, and analog devices for automotive applications have increased the required implant energies into the range of 4-8 MeV. Characterization of the ion stopping and channeling behavior of common dopants into silicon at these energies is therefore important.

We present SIMS data and analysis for dopant profiles implanted at energies up to 15 MeV. We focus on arsenic and boron, which are widely used for very high-energy implants into and adjacent to the photodiode region of CMOS image sensors to improve quantum efficiency and isolation. To avoid lateral shifts, shadowing effects, and to use channeling to increase ion penetration depth, the majority of high-energy implants are performed at normal incidence or low beam tilt angles. Precise alignment and control of ion beam angles is therefore extremely important.

SIMS analysis of profiles were performed on (100) Si-wafers implanted with MeV-range energies using singly or multiply charged ions of As and B. Certified wafers with a slice angle offset of <0.05° from <001> were used. The surface offset of the wafers were verified and accounted for using the TW V-curve method. We studied arsenic profiles implanted in silicon at energies of 8-15 MeV at the <001> axial channeling condition and at low tilt angles using 0.05° angle increments. A similar test was performed for boron at 3.6 MeV (Fig.1). As expected, very high energy dopant profiles are highly sensitive to ion beam incident angles and require angle alignment and control relative to the wafer crystalline plane better than 0.05° [1].

For implantations with incidence near but not at the <001> axial channel, wafer twist angle is important because the resulting profile is a combination of both <001> axial channeling and (110) planar channeling. Comparing SIMS profiles from 0° and 22° twist angles at low tilts shows a significant, non-linear contribution of planar channeling that affects the arsenic profile shape. SIMS profile comparisons for different beam currents and implanted doses will also be presented and discussed.

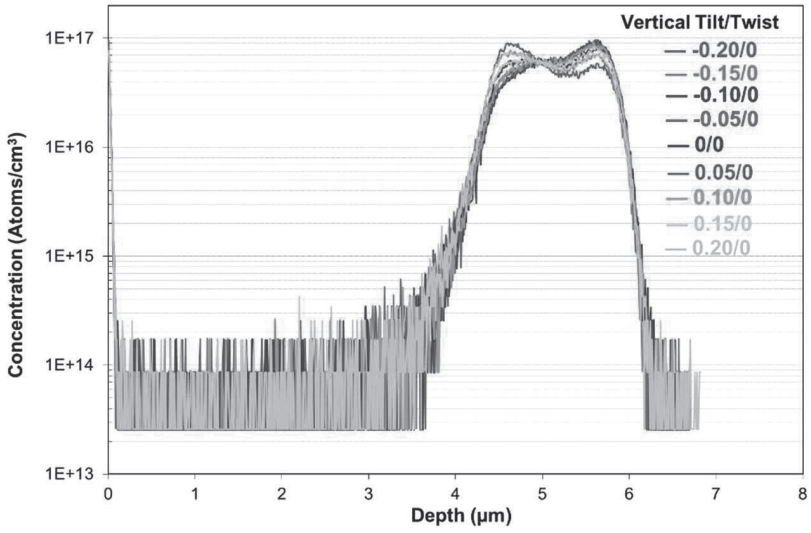

Fig.1 Boron implanted in Si (100) at an energy of 3.6MeV and dose $1x10^{13}$ at/cm^2 at tilt angles from -0.2° to 0.2° with a 0.05° tilt angle increment.

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Neutron Radiation due to High Energy Boron Ion Beams

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Axcelis' next generation high energy implanter, the Purion XEmax, can achieve ultra-high energy Boron, Arsenic and Phosphorus beams. The fabrication and future development of leading-edge CMOS image sensors are likely to require high energy Boron ion beams, in an energy range of about 1 to >=5 MeV. At these energies nuclear fusion can occur due to quantum tunneling which results in neutron radiation as was discussed in a previous 2008 study [1]. This study examined one particular fusion reaction, the $^{12}C(^{11}B,n)^{22}Na$ reaction for 6 – 10 MeV Boron beams reacting with graphite liners commonly used in ion implanters. However, this work found that Boron beams interacting with targets previously implanted with Boron can result in much higher levels of neutron radiation due to the greater cross-section of the $^{11}B(^{11}B,n)^{21}Ne$ fusion reaction. Neutron radiation is a serious safety concern, because unlike x-rays, neutrons are much more difficult to safely manage. This paper discusses in detail, the neutron dose rates for Boron energies for 4 – 8 MeV, various beam currents, target materials (C, Si, BN and pre-implanted graphite), angles of incidence, neutron detectors as well as shielding materials.

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Assessment of a 2MeV Li+ Ion Beam Resolution by means of the Ion Beam Induced Charge Technique.

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MeV ion beams are an appealing and versatile tool for the modification, functionalization and analysis of solid state materials. In the last decade, single-defect engineering relied on the controlled introduction of individual dopants by ion implantation [1] and the functionalization of materials at the nanoscale [2] have significantly benefited from the steady improvements in the focusing and collimation of ion beams. Indeed, the availability of tools for the accurate control on the beam size and its resolution become crucial in processing involving the employment of MeV beams which spot sizes approach the nanometre scale. So far, STIM (Scanning Transmission Ion Microscopy), RBS (Rutherford back-scattering) and PIXE (Particle Induced X-ray Emission) are the main techniques commonly implemented by the scientific community. Since they rely on the imaging of patterned standards to access the beam resolution [3], e.g. TEM grids, a dedicated reference standard typically different from the sample to be processed is required. Moreover, a separate measurement system and ion currents ranging from nA (as for PIXE and RBS) to fractions of fA (as for STIM or other single-ion detection technique) are needed.

To overcome these possible limitations to the accuracy of the beam size estimation at sub-μm scales and in the perspective of practical and automated functionalization processes when high positional accuracy and precision are demanded, we propose here a new method for the evaluation of the resolution of low energy micro and nano-beams. Specifically, the sample target itself is exploited as a diagnostic tool for the real-time assessment of the ion beam resolution. We report a new concept for an ion beam spot size monitor based on a custom Si photodiode nanomachined via FIB milling. The proposed case study assesses the possibility to gain spatial information on the size of a 2MeV Li+ ion micro-beam through the realization of a dedicated Ion Beam Induced Charge (IBIC) experiment. Charge collection efficiency (CCE) measurements on the machined structures revealed a spatial correlation in the induced charge pulse amplitudes and the micromachined structures, which were used to estimate the resolution of the probing beam. Numerical simulations based on the Shockley-Ramo-Gunn model were performed to validate the interpretation of the results in terms of the effects of FIB nanomachining on the device charge transport properties.

Despite recent approaches of the scientific community have proposed to employ the target samples themselves as resources for single ion detection with position sensitivity [4], their application as integrated beam diagnostic tools has not been explored yet. Therefore emerging fields such as deterministic implantation, micro radiobiology, and ion lithography, benefiting from beam spot sizes below the micrometer scale could benefit from the proposed technique, which has the potential to offer an effective method to routinely evaluate the resolution of ion microbeams processes and experiments.

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Metrologies to Study Ion Implanted Semiconductor Materials

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As ion implantation technology for semiconductors evolved, new metrologies to help its progress needed to be developed in parallel. Some of the current metrologies owe their present sophistication to this evolution. The one technique which probably underwent the most development was Secondary Ion Mass Spectrometry (SIMS). New SIMS instrumentation needed to be developed to measure very low dose and ultra-shallow implants. High dose shallow implants led to changes in matrix composition to stoichiometries that required new SIMS quantification formulae. Several complementary analytical methods needed to be employed to further improve the accuracy of SIMS data.

Over the years, many new metrologies were also developed to investigate the physical properties of ion implanted materials. Advances in electron microscopy made high resolution crystallinity analysis of semiconductor materials easier over the years, in combination with accelerator techniques such as RBS. Atom Probe Tomography became available to provide a 3-dimensional atomistic view of these materials. The newly developed method of Differential Hall Effect Metrology (DHEM) complements SIMS, as it measures active dopants in the top 100nm with <1nm resolution.

The complete study of materials modified by ion implantation requires a combination of the above techniques, with the occasional use of others, such as XPS and XRD. Analytical approaches utilizing some or all of the above will be discussed in detail this presentation.

Lateral Mapping of Damage Patterns in Plasma Immersion Ion Implanted Silicon

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It is highly desirable to monitor residual damage in silicon originating from plasma immersion ion implantation doping (PLAD) both for pre- and post-annealed states. For fine structure highly doped shallow junctions annealing is performed by subsequent energetic short laser pulses according to a predetermined laser exposure pattern. It is straightforward to optimize key parameters governing the laser annealing process, e.g. laser beam fluence and the applied geometrical configuration: the use of overlapping or non-overlapping subsequent laser exposure steps.

In this work 2 kV BF_3 PLAD has been performed in the dose range 5e14-1e16 cm^{-2} on p-type (100) Si wafers provided by Ion Beam Services (IBS). PLAD was followed by pulsed laser annealing applied in both overlapping and non-overlapping configuration and with different laser fluences in the range 0.4-0.6 J cm^{-2}. The effect of annealing has been analyzed by Semilab characterization techniques: photo-modulated reflectance (PMR) and micro-photoluminescence (μ-PL). Combination of these methods provides effective manufacturing process control and gives valuable information on residual damage level, extended defect formation and carrier recombination processes [1-3].

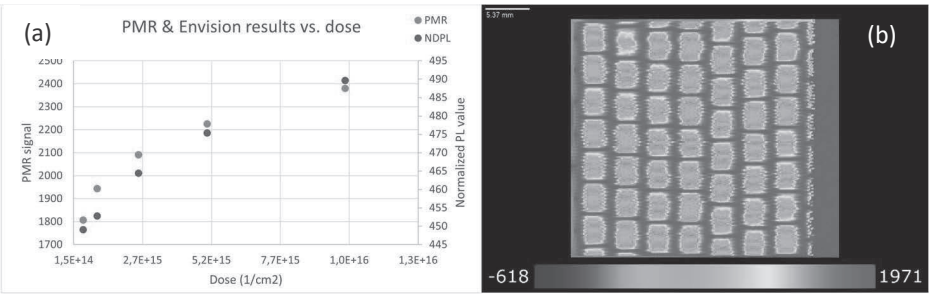

Fig. 1 (a) PMR signal and normalized defect PL (NDPL) intensity vs. PLAD implant dose; (b) PMR map measured on PLAD implanted Si after laser annealing performed in non-overlapping configuration.

In addition to the obtained excellent correlation between PMR signal and ion dose in as-implanted areas (Fig. 1a), significant differences in the material properties have been found between the overlapping and non-overlapping annealing configurations as well. Furthermore, for the non-overlapping case, notable variation of the surface layer properties has been observed in the centre and nearby the edge of the annealing laser spot, as well as in the gaps between adjacent spots (Fig. 1b). PMR features high enough spatial resolution to detect lateral gradients in the annealed samples on a significantly smaller length scale than the annealing laser spot size and provide valuable information on sample homogeneity vs. PLAD and annealing process conditions. The normalized defect PL (NDPL) intensity follows monotonous trend with PLAD implant dose. In addition, μ-PL patterns show striking differences in extended defect formation as a function of the annealing laser power density, i.e., at 600 mJ laser pulse energy extended defect formation can be observed, while for lower pulse energies extended defects were not detected. The observed trends for damage formation and defect recovery are supported by the results of complementary measurements: micro-beam spectroscopic ellipsometry (μ-SE), and high-resolution wafer mapping with Raman scattering spectroscopy.

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Measuring sub-nm Activation Profiles in very Highly Doped Semiconductors

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Carrier concentration and mobility values define the quality of a semiconductor layer and resulting device performance. The commonly used techniques to determine these parameters are 4-point probe and Hall effect measurements, which yield Hall mobility (μ_H) and carrier concentration (n) values for the whole film. These measured bulk values can be used for correlating process conditions and film attributes **only if** the mobility and carrier concentration are uniform through the measured film. If the mobility and/or the carrier concentration vary through the film, then the bulk mobility measurement gives an effective mobility value and an effective carrier concentration may be derived using 4-point probe data.

$$\mu_{H\,eff} = [\int n(z)\,\mu(z)^2\,dz\,] / [\int n(z)\,\mu(z)\,dz\,] \qquad (1)$$

$$n_{\,eff} = [\int n(z)\,\mu(z)\,dz\,] / [\int dz\,][\mu_{H\,eff}\,] \qquad (2)$$

As can be seen from the equations above, depending on how the mobility and the carrier concentration values vary through the thickness of the film (in "z" direction), the bulk effective values obtained from these measurements cannot define the true characteristics of the film and therefore can be very misleading. Recognition of the need for depth profiling electrical parameters gave rise to development of techniques such as Scanning Spreading Resistance Microscopy (SSRM) and Electrochemical Capacitance-Voltage (E-CV) techniques [1, 2]. However, one limitation of these approaches is the fact that they measure either the resistivity or carrier concentration values, without providing mobility depth profiles. This necessitates assuming a mobility value for the thin-film, which is problematic for various reasons. The silicon mobility models are based on a 1981 publication [3], while the germanium models are mostly taken from a 1961 paper [4].These models may not be absolutely relevant to materials produced today using modern processing approaches, which may introduce very high concentrations of dopants in the surface region of the films and utilize non-equilibrium approaches such as laser annealing. Furthermore, models do not directly expand to include new materials such as Si-Ge alloys with varying amounts of Ge. There is also limited electrical data for thin films of III-V materials grown by different approaches. Therefore, a technique that can directly measure depth profiles of carrier concentration and mobility through layers at high depth resolution is highly valuable. Differential Hall Effect Metrology (DHEM), which is based on the Differential Hall Effect (DHE) method provides depth profiles of all critical electrical parameters through semiconductor layers at nanometer-level depth resolution [5].

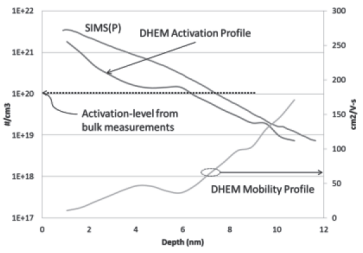

Figure 1: Highly doped implant sample SIMS, DHEM Activation and Mobility Profiles. Activation-level from bulk measurements is also shown.

In this paper we will present data on DHEM depth profiling of very highly doped silicon materials (>1e21/cm3 dopant concentration levels, see Fig 1) to demonstrate crucial activation information at sub-nm resolution. Samples considered are highly doped Phosphorus and Arsenic-implanted samples, and epi-grown layers. Extensive post-DHEM metrology (using TEM and SIMS analysis) will also be presented demonstrating control and precision of DHEM data.

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NS-Pulsed Melt Laser Annealing for Advanced CMOS Contacts

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Nanosecond-pulsed (ns) laser annealing (LA) enables melting of ion-implanted (I/I-ed) semiconductors to facilitate the removal of crystal damage and activate the dopants in a metastable state. In this work, we review our recent progress on the challenge of reducing the contact resistivity for advanced CMOS devices.

The melting by ns LA of a semiconductor substrate partially amorphized by I/I follows different regimes. In Explosive Melting (EM), a thin liquid layer of a ~2-10 nm thickness travels in the depth direction.[1-2] In Secondary Melting (SM), the melted layer forms at the surface and extends downward.[3] Both EM and SM layers stopping within the amorphized layer result in polycrystalline regrowth. If the SM layer reaches the bottom of the amorphized layer, then monocrystalline regrowth becomes possible.[4-5] However, a high doping concentration and stress relaxation might induce stacking faults and dislocations, respectively. Active carrier concentration must be elevated near the surface to lower the contact resistivity (ρ_c). Elements like antimony (Sb) and gallium (Ga) show surface segregation during ns LA induced solidification and are therefore interesting for n-type doping in Si and p-type doping in SiGe, respectively.[4-5]

We observed monocrystalline regrowth when fully melting the amorphized layer in Sb I/I-ed Si and Ga I/I-ed SiGe. However, stacking faults and dislocations remained. To suppress the growth of stacking faults and stress relaxation, the amorphization thickness was reduced. Cold I/I was also selected to reduce the crystal damage of the non-amorphized layer. The Sb and Ga I/I were done in more realistic epilayers such as *in situ* phosphorous doped Si (Si:P) and *in situ* boron doped SiGe (SiGe:B), respectively. After the full-melt regrowth, the remaining defects were unobservable by cross-sectional TEM. The ρ_c value was measured by MR-CTLM.[6] For the Sb-implanted Si:P, the lowest ρ_c was 2.1 (±0.5) × 10^{-9} ohm.cm^2. This value is equivalent to the one obtained without Sb I/I, meaning that the Sb surface segregation was so strong that almost all I/I-ed Sb were lost from the substrate by outgassing. To avoid this, a capping layer may help. For the Ga-implanted SiGe:B, the lowest ρ_c was 1.3 (±0.5) × 10^{-9} ohm.cm^2. Although partial Ga loss due to outgassing might have happened, this value meets the target for the 5 nm technology and beyond.[7] To further improve ρ_c, deep level substitutional sites (typically known for arsenic in Si)[8] might have to be reduced. Indeed, the 1/C^2-V curvature and discontinuity found in Electrochemical Capacitance Voltage Profiling of the Ga I/I-ed SiGe imply their presence.[9] In Fig. 1, solidification velocity (v_s) strongly affects the activation,[5] and a theoretical prediction[10] suggests having a higher v_s in a typical melt LA solidification ($\sim 10^{-1} < v_s < \sim 10^{1}$). For N14 FinFETs, the contact epi volume becomes negligible compared to the substrate, so that strong heat dissipation enhances v_s.[11]

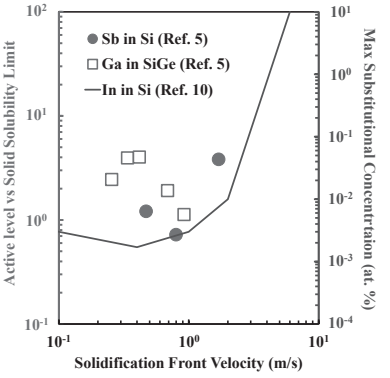

Fig. 1. Active level and max substitutional solubility evolution as a function of v_s.

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The work covered by LASSE and imec in this paper was supported by the IT2 project. This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 875999. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Netherlands, Belgium, Germany, France, Austria, Hungary, United Kingdom, Romania, Israel.

The detail analysis of behavior of heavy metals in 4H-SiC

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Silicon Carbide (SiC) power device has been attracting many attentions in terms of its high breakdown electric field strength and large bandgap energy [1]. The heavy metal contamination can cause harmful effects such as the degradation of gate oxide reliability and increase in junction leakage current. However, there have been only few reports of the behavior of metal ions in SiC. [2] We investigated the behavior of heavy metals in SiC in detail.

Heavy metal was intentionally introduced by ion implantation into 4H-SiC. To clarify the effect of implantation damage, Al^+ and Ge^+ ion were implanted at room temperature (RT) and 500 degree C (HT). The implantation depth and dose for Al^+ and Ge^+ were adjusted at 50 nm and 5.0 x 10^{15} ions/cm^2, respectively.

Fig. 1 shows SIMS depth profiles of Fe in samples with the (a) Al^+ and (b) Ge^+ implantation. All samples were annealed at 1700 degree C for 30 min in Ar ambient with carbon cap layer. The result of sample without implantation is also shown. Fe atoms easily diffuse into SiC epitaxial film during high temperature annealing. It should be noted that the quite different behavior of Fe atoms was observed if co-implantation was carried out. Moreover, Fe diffusion entirely depends on the temperature during ion implantation. In the case of HT implantation, Fe diffusion toward the surface is suppressed. The diffusion coefficient of Fe would become smaller due to the formation of Fe-Al or Fe-Ge complex. Especially, almost no Fe diffusion was observed in the case of HT Ge^+ implantation. In the case of RT implantation, Fe diffusion was enhanced comparing with that of HT implantation. We speculate that implantation related point defects such as vacancies, interstitials, and defects complex enhanced the diffusion of Fe-Al or Fe-Ge complex. The large amount of point defects is generated during RT implantation. Furthermore, Fe atoms seem to be captured at the EOR defects region. It has been found that the Fe diffusion was affected by defects and implanted ion species. We will show and discuss the behavior of other heavy metals such as Ti and Ni at the conference.

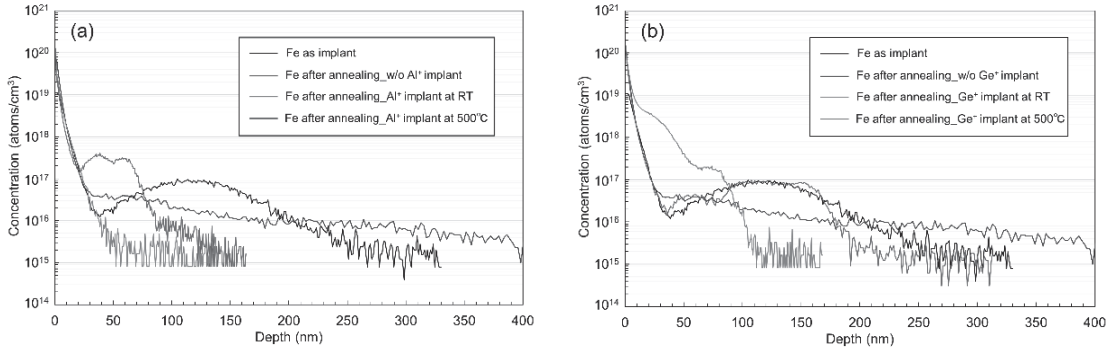

Fig. 1 SIMS depth profile of Fe in the case of (a) Al^+ and (b) Ge^+ implantation

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Comparative Evaluation of Indirectly Heated Cathode DC Ion Source and Inductively Coupled Plasma RF Ion Source at High Current Ion Implanter.

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Abstract

Ion implanters, commonly used in memory semiconductors, use DC ion source to generate impurities ion. RF ion sources are less widely used in ion implanters for memory semiconductors due to reduced ionization rates at low gas flow and high vacuum. In this study, an inductively coupled plasma (ICP) RF ion source applicable to the high current ion implanter for memory semiconductors was developed and physical properties were identified. The current, voltage characteristics, and ion density of DC and ICP ion source were compared using Langmuir Probe. Extraction current, beam current, and atomic mass unit(AMU) spectrum of Ar, PH_3 and BF_3 gas were evaluated on an AXCELIS OPTIMA HDx. The contamination level of the ICP ion source was checked using inductively coupled plasma mass spectrometry (ICPMS). Secondary ion mass spectrometry (SIMS) was used to compare the characteristic of the dopant generated from the ICP RF ion source according to the depth of implantation into the wafer with that of the DC ion source. Finally, two recipes of high current implantation process were performed using the ICP ion source in AXCELIS PURION H, a DRAM device production equipment, and a yield of equal or higher was ensured and its applicability was confirmed.

Keywords – Ion Source, High Current Ion Implanter, RF Plasma

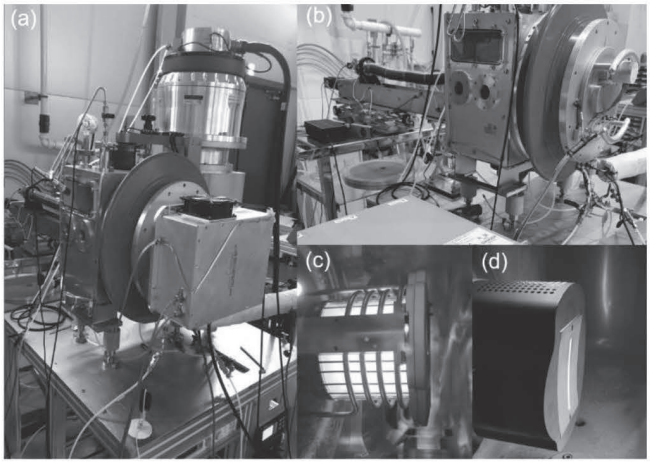

Fig. 1. Ar ignition test chamber with Leybold “MAG-W 3200” turbo pump. (a) installed RF power, (b) installed DC power, (c) Ar plasma at ICP ion source, (d) Ar plasma at DC ion source

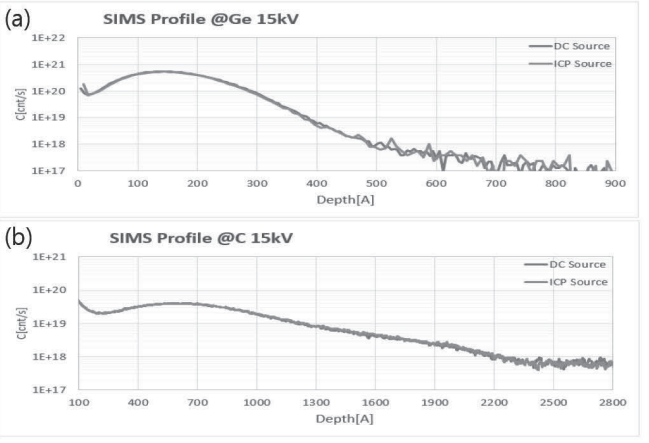

Fig. 2. ICP and DC SIMS profile results of (a) Ge15kV, (b) C15kV.

Risk of Neutron Generation with Implantation of Light Ions

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ABSTRACT – A neutron detection study was performed on a high energy ion implanter with an ion source tuned to accelerate light ions from AMU 1 to 4. For all species, under specific conditions of beam impact location and placement of the detector, for the beam current range and energy range regularly used in production, the radiation levels from neutron producing reactions were found to be well under the legal US Occupational Safety and Health Administration (OSHA) limit of 0.570 mrem/hr. For the highest energy and beam current, the radiation levels were observed to be above the implanter maker specification (maker spec) of 0.054 mrem/hr, and the 0.010 mrem/hr recommended limit by the International Commission on Radiological Protection (ICRP) [1]**. Extra care must thus be used when performing implantation of light ions in semiconductor compounds.**

The recent increased interest in the use of light ions such as $^{1}H+$, $H_2+/^{2}D+$, $^{4}He+$ and $^{4}He++$, for implantation into silicon-based semiconductors and especially into compound semiconductors has led us to investigate potential risk for neutron producing reactions associated with these processes. These light ions are showing a better damage control in dose and depth without any detrimental charge doping, along with a larger process window margin than heavier ions.

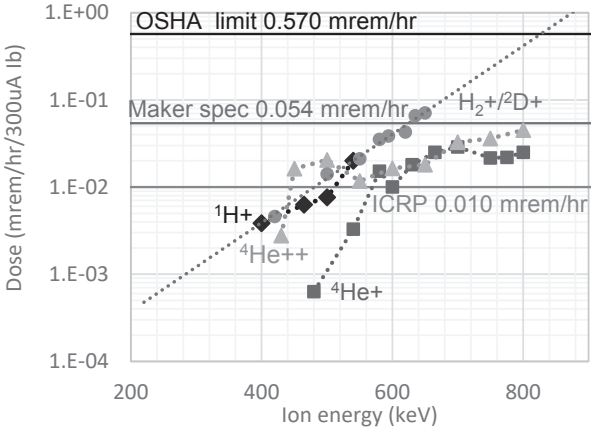

Figure 1- Relative neutron dose as a function of energy of incoming ions, normalized by 300 uA of beam current, and being produced by light ion implanted into the resolver of high energy implanter.

However, for these light ions constituted of a few nucleons less strongly bound than heavier ions, the likelihood of a nuclear reaction when accelerated and colliding with a target is higher. They indeed exhibit the largest cross sections for neutron producing reactions [2] [3] [4] [5]. In typical ion implanter tools, there are a few places such as the mass analyzer, the Faraday flag also called resolver, the wafer to be implanted, which constitute point of impacts for the ion beam and are potential source locations for such neutron producing reactions to occur. In addition, these points of impact are usually made of graphite which not only by itself constitute a producing target as being made of carbon ($^{12}C/^{13}C$) but also due to its high absorbance characteristic, accumulate different type of ions when the tool is used with various ion species, *e.g.,* $^{10}B/^{11}B$. These absorbed ions along with carbon present very high absorption cross sections and constitute target for subsequent light ions to strike and potentially generate neutrons [6].

The energy thresholds for such reactions can be as low as 0 MeV for some particles like deuterium, $^{4}He+$ and $^{4}He++$, on atom targets like ^{9}Be, ^{10}B, ^{11}B and ^{13}C [3] [7] [8] [9] [10]. This paper outlines a few characteristics of some of these reactions and the potential risks associated with them.

In conclusion, special considerations and care should be followed for the implantation of light ions into semiconductor compounds. One of them is the controlling of the accumulation of ions prone to generate neutrons on the tool parts by implementing a regular and thorough polishing and cleaning of any strike part.

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Ion Implantation and activation of Aluminum in bulk 3C-SiC and 3C-SiC on Si

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Emerging wide bandgap semiconductor devices such as the ones built with SiC have the potential to revolutionize the power electronics industry through faster switching speeds, lower losses, and higher blocking voltages, which are superior to standard silicon-based devices. Besides the widely used 4H-SiC, the cubic polytype 3C-SiC, with 2.3 eV band gap, has interesting features such as possibility to be grown on a silicon substrate, a reduced density of states at the SiC/SiO2 interface, and a higher channel mobility, characteristics that are ideal for its incorporation in metal oxide semiconductor field effect transistors. However, realization of defect free bulk 3C-SiC wafers is very challenging and p+ doping and activation mechanisms using ion implantation followed by thermal annealing are not well-known.
Within the framework of the European R&D project CHALLENGE, we studied ion implantation of Aluminum on bulk 3C-SiC as well on EPI grown 3C-SiC on Si followed by furnace and/or laser anneal. For 3C-SiC on Si, results using long furnace anneal at temperature < 1400°C as well as laser anneal are presented. SIMS, ECV, TLM and VdP characterization methods have been used to study the chemical and active dopant profiles as well as sheet resistance and contact resistance. The effect of doping concentration and the interest of laser annealing for contact resistance improvement are discussed. For bulk 3C-SiC, results using higher temperature annealing (1700°C) are presented

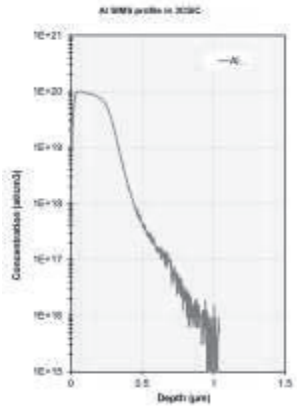

Fig.1 : Example of Al SIMS profile obtained on a 3C-SiC on Si substrate using multi energy ion implantations of Al^+ at 600°C to obtain a 200 nm box profile with concentration of 1 × 10^{20} Al/cm^3

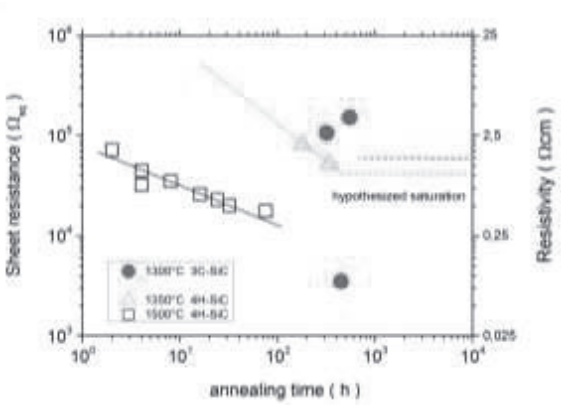

Fig.2 : Sheet resistance of 200 nm, 1 × 10^{20} Al^+ ion implanted 3C-SiC and 4H-SiC layers versus annealing time after 1300-1350-1500°C treatments with C-cap

Acknowledgment. This work has been supported by the European project CHALLENGE (Call: H2020-NMBP-2016-2017, grant. agreement 720827).

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Fabrication of nano- to micro-scale optical structures in silica

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We have studied the changes in the optical properties of fused silica (Infrasil) using the spot-by-spot MeV ion implantation of metallic elements. In previous work we have reported on how to place well-defined metallic nanoparticle populations in this material at particular depths, with tailored plasmonic absorption characteristics, changing the index of refraction of the implanted substrate in a pre-defined manner. The ultimate goal of this project is to use focus ion beam to fix the embedded optical roadmap into any transparent host. To achieve such goal, we studied the use of focused MeV ion beams of 0.785 MeV Ag and 1.450 MeV Au into silica, with spot sizes ranging from a few hundred micrometers up to 2mm.

In one investigation, highly focused ion beams were allowed to impact the transparent material in a stationary spot, until the desired fluence was delivered, after which the substrate was moved stepwise laterally to observe the minimum steps size which would produce discrete embedded structures observable by a 3D optical microscope.

In a separate investigation, using larger spot sizes, we moved the substrate stepwise in small increments across an 8mm x 8mm area, calculating the total fluence delivered in each overlapping spot, to produce a uniformly implanted area. Fluences were confirmed using Rutherford backscattering spectrometry (RBS) to produce a uniform total implantation doses of Au, Ag, and (sequentially) Au + Ag ranging from $10^{16}/cm^2$ to $10^{17}/cm^2$. The effects of this high dose spot-by-spot method on the optical absorption were then compared with traditional raster scan implantations, in which the beam is swept over the entire area quickly, and the entire area is implanted at once at a slower implantation rate. Using optical absorption photo spectrometry, we assessed the optical changes in the material and evidence of Au and Ag nanocluster formation both as-implanted and after subsequent annealing at temperatures up to 1100 C. We have observed, specifically in spot-by-spot Au implanted silica, evidence of a quadrupole interaction which produces widening of the Au nanocluster absorption band beyond 530nm, and which has been seen in past studies using traditional raster scanning followed by annealing. We also report on an ordered change in the index of refraction of the host observed using 3D microscopy; this ordered change appears to be correlated with the small lateral stepwise increments using in the implantation process, which appear to have induced 3D embedded optical structures.

Oral or Poster: No preference
Proposed sessions:
Preference

1. Metrologies for Implant/Doping and Annealing Processes
2. Implant/Doping Technologies and Processes

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IMPHEAT-Ⅱ, a novel high temperature ion implanter for mass production of SiC power devices

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Silicon carbide (SiC) wafers are widely used for the production of power devices. More and more SiC based power devices are being implemented for producing power modules used in electric motors, bullet trains, solar panels, home electronic appliances, etc. In order to meet all of these needs, power device makers require higher throughput tools to manufacture the devices more economically. We developed a new high temperature ion implanter having 3 times higher mechanical throughput and 2 times higher effective throughput @ 500degC compared with our former tool IMPHEAT. We named it IMPHEAT-Ⅱ, the second generation of high temperature ion implanter—for SiC based power devices.

Fig.1 is a photo of IMPHEAT-Ⅱ. The basic layout has not been modified from IMPHEAT. Compared to IMPHEAT, IMPHEAT-Ⅱ has the following improvements, (1) By introducing Hydrogen co-gas, we were able to increase beam current 2 times higher with much more stable condition for Al. (2) The wafer handling system has been improved drastically as well. A preheating unit has been added to the Load-Lock chamber 1 (L/L1) to reduce the wafer heating time on platen. Improvements have also been implemented to make it possible for the vacuum robot to carry out multi-tasks and increase the mechanical throughput. Wafers are cooled down in Load-Lock chamber 2 (L/L2) after being implanted, and L/L2 has a much quicker and stable wafer cooling down process. These improvements have increased the mechanical throughput of IMPHEAT-Ⅱ 3 times higher than that of IMPHEAT.

As a result from these improvements, IMPHEAT-Ⅱ has the highest effective productivity for SiC power device manufacturing requirements.

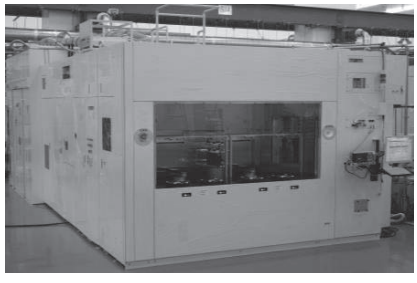

Fig.1. A photo of IMPHEAT-Ⅱ

Electrostatic ion implant chuck with fast declamp response through charge control

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Residual charge buildup on the surface of an electrostatic chuck and the contacting wafer is a major factor impacting throughput rates and performance of implant processes. To address this issue a method to facilitate charge transport at the chuck's surface is needed, allowing to drain the residual surface charge in an efficient way. This is typically accomplished by tuning the electrical conductivity at the surface of the chuck, typically by means of moderately conductive surface coatings. However, there is a balance between increased surface conductivity that leads to improved charge dissipation and the conductive layer directly interfering with the wafer clamping performance, because of electrostatic force being increasingly more coupled with this conductive surface coating, instead of the wafer.

We will be presenting an optimized charge control solution**,** which enables very efficient charge transport with minimal interference of the clamping action. We will be discussing the surface charge transport mechanism and the physics supporting this design solution. Furthermore, we will be illustrating various design considerations and configurations that are tailored to maximize clamp force and reduce wafer sticking. We will also present a few very specific design examples of electrostatic chucks with this new charge control concept and discuss their performance.

Format: poster presentation

Topic field: Advanced Implant Equipment

Keywords: electrostatic chuck, wafer sticking, wafer clamping

New control system of the multiple filaments in the large ion source for ion doping system iG6 Ver.2

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The ion doping system “iG6” is used for advanced applications of Low Temperature Poly-crystalline Silicon Thin Film Transistor (LTPS-TFT) such as system-on-glass devices and OLED displays. The large ion source used in iG6 has multiple filaments. Thermal electrons are emitted from each filament, and collide with the material gas to generate plasma. Ions in the plasma are extracted through an electrode system with multi slits.

The target beam profile is measured by multiple Faraday cups and the uniformity of the ion beam can be improved by adjusting the current of each filament which can control a certain region of the target beam profile. Our conventional method of the filament control uses this one to one correspondence between each filament and corresponding target region.

In the plasma production chamber of multi-cusp ion source of iG6, the magnetic field strength is higher than that of typical multi-cusp ion sources and the plasma drift occurs easily. Therefore, the difference of plasma density around each filament occurs. It causes the difference of the etching rate and the variation of the resistance between filaments. And in the conventional control system, each filament current has to be changed frequently to keep good beam uniformity.

Figure.1 shows the change of the variation for multiple filament resistances and the beam uniformity keeping the averaged target beam current density constant using the conventional method. Using the new method, the result is shown in Figure.2. Compared to the conventional method, the filament life was prolonged approximately 1.5 times and the good uniformity of the ion beam was maintained.

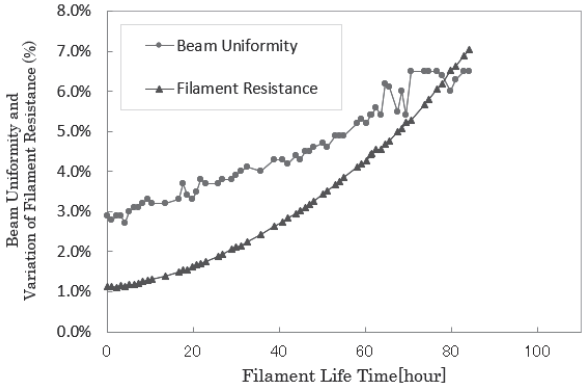

Fig1. Result of the filament current control by the conventional method.

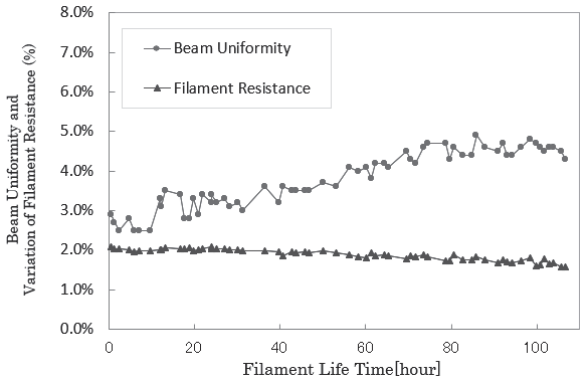

Fig2. Result of the filament current control by equalizing each filament resistance.

ECR ion source with wide dynamic range of beam current

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An Electron Cyclotron Resonance (ECR) ion source with wide dynamic range of beam current has been developed for medium current ion implanter. Ion implantation technology for analog devices requires metal contamination free process. As the ion source for medium current ion implanters, the ion sources using thermal electron emission for plasma generation such as indirectly heated cathode (IHC) and Bernas type ion source are currently mainstream. Using thermal electron emission these ion sources can produce beam current widely. These ion sources can produce beam current with wide range for medium current ion implanter which beam currents are from a few micro amperes to several milliamperes.

One of the advantage of ECR ion source is that it is possible to generate plasma without using metal electrodes. General ECR ion sources use waveguide tubes to supply a high power microwave to plasmas. It enables to obtain high beam current of multiply charged ions, while maintaining plasma with a small microwave power is difficult. The range of the beam current is narrow and the precise control of the beam current is difficult.

Newly developed ECR ion source can maintain plasma in a wide dynamic range of beam current, by introducing microwave into the plasma chamber with an antenna. As the beam current changes linearly with the input power, it is easy to control the beam current. Figure 1 shows the B+ beam current characteristics as a function of micro wave power using the developed ECR ion source.

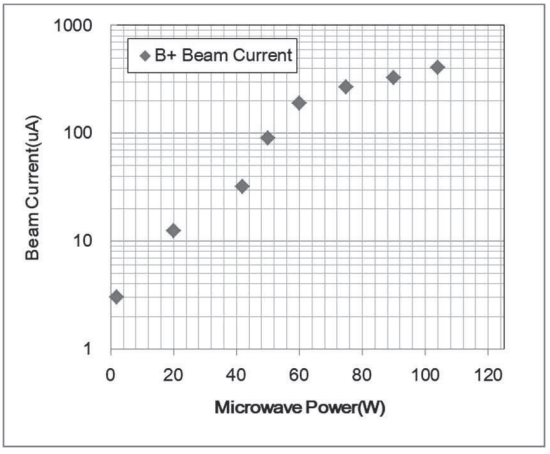

Fig. 1 B+ beam current characteristics as a function of microwave power

Linac Simulation with Dataset Generator

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A dataset generator was developed for Axcelis' higher energy ion implanters, specifically for the Purion XEmax, which employs two linear accelerators (LINACs). It has the advantage that it doesn't rely on previously created datasets and can be applied to any random species and energy thus greatly speeding up the development of new recipes. At its core it uses a LINAC simulation to verify that the generated LINAC parameters achieve the desired particle energies with acceptable beam transmission. The LINAC simulation is an in-house written particle dynamics code that uses the equation of motion for alternating electric fields in the RF range. It generates virtually identical energy spectra as Los Alamos' Parmela code, but runs faster. The LINAC simulation works equally well for low and high AMU species, as well as various charge states and energies. The dataset generator on the other hand works best for a mass-to-charge ratio (m/q) for which the respective LINAC drift tubes were designed for (typically m/q < 33). As a first step, it automatically generates roughly correct RF amplitudes and phases based on the desired final energy and typically achieves >30% transmission. As a second step a fine tune algorithm can be employed such as the Downhill Simplex Method in Multidimensions to achieve higher beam transmission. The first step takes about 1 min and the second step typically 3min. In some cases, the fine tune step is not necessary. When the dataset is applied to an actual ion implanter, all that is required for implementation is that it results in some transmission at the desired energy. Only ~10% transmission is sufficient since one can improve the transmission with the available standard tuning routines (buncher, quick or full tune). In addition, it will generate equal RF amplitudes (except for the buncher), so the electric stress on each resonator is kept to a minimum. In this paper, we detail the model for this simulator and show its effectiveness at generating real datasets for accelerating ions through the LINAC.

Improvements Enabled in SiC Power Devices by Advancements in Ion Implantation Hardware

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Ion implant constitutes roughly 30% of all wafer-fab equipment capital expenditure for silicon carbide (SiC) fabrication facilities. This is primarily because dopants such as aluminum do not migrate in SiC substrates when annealed, requiring several “graded” implants at varying energies to create box- profiles. Many of these implants are high enough in dose to cause damage to the SiC substrate that cannot be fixed during the activation anneal. In order to minimize this damage many high dose (and moderately high dose) implants are done at elevated temperature – typically at or about 500 C. Significant deviations from this temperature can lead to hot, or cold spots on the wafer which will affect the final yield from that wafer. Advantages of hot implant for SiC relative to room temperature implants has been previously published (figure 1). It is therefore critical to elevate the wafer temperature to the required setting uniformly and repeatably. This is typically done with the wafer clamped to a hot platen in the “end-station” of the implant tool. The wafer can be mechanically clamped to the platen using edge tabs made of appropriate temperature capable material. However, this mechanical clamp degrades over time due to repeated beam-strike and leads to particle excursions as well as expensive and lengthy preventative maintenance to replace these clamps. Additionally, mechanical clamps do not “couple” the wafer adequately to the hot platen, i.e., only allow radiative heat transfer since the SiC wafer bow does not allow backside gas flow, requiring the platen to be as much as 200 degrees hotter than the required wafer temperature. This wafer bowing effect can also cause non-uniformity in implant profile These issues are resolved on the Applied Materials VIISta® SiC implant tools by using an electrostatically clamped hot platen (figure 2). This Thermion® platen clamps the wafer flat against the platen, which is a significant advantage for SiC wafers that may have a large bow or warp (figure 3). Once clamped, high pressure backside gas flow is enabled to thermally “couple” the wafer to the hot platen. Due to this convective and conductive coupling the platen needs

Ion implanter beam optics design using global optimization techniques

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When designing components of the optical train of an ion implanter beamline, the methodology comprises defining desired beam properties, selecting the type of optical component, a combination of first and second order optics modeling using analytical or numerical models, and subsequently, ion beam modeling using field and ray-tracing solvers [1]. The design goal is typically to optimize implanter operation and performance parameters, such as ion beam transmission and angle distribution, while staying within practical constraints and compliance to design standards. The optimization needs to start with a judicial choice of dimensions and parameters for an initial design, either based on a previous design or the optics designer's experience.

In this study, we explore applying modern global optimization techniques to beam optics design, made feasible by the progress in computation speed of modern workstations. Such an approach eliminates the need for an initial candidate design and is more likely to avoid local optima in the design parameter space. Setting up a global optimization requires a fully parametrized geometry, where all physical and operating parameters are flexible within a constrained space, and a cost function describing the desired properties to be optimized. We illustrate the technique using a genetic algorithm to optimize the geometry of a bending dipole magnet for point-to-parallel optics with prescribed ion beam density control [2]. The magnet geometry is described by a set of parametric edges defining the shape of pole pieces, and the coil current is variable to ensure parallelism of the ion beam. The cost function of the optimization is calculated from ray-traced beamlets for each combination of design parameters, and the genetic algorithm selects solutions with highest beam quality and desired beam density. The algorithm converges after ~25 generations to multiple solutions. Measurements on a prototype magnet agree well with beam parameters predicted by the model.

[1] see, for example, Wollnik, H. "*Optics of Charged Particles"*, 2nd Ed., Elsevier (2021)
[2] US Pat. 11,037,754

Purion XEmax, Axcelis Ultra High Energy Implanter with Boost Technology

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The competition for improved red and IR sensitivity within the CMOS Image Sensor (CIS) industry is expanding the performance requirements of Ion implanters. The desired energy range well above 10 MeV was once only considered for nuclear physics experiments but is now needed for advanced CIS devices. The sensitivity of CIS device to metals contamination calls for even tighter control of implant purity. Additionally, the increased use of channeled implants has placed stricter controls on beam angle uniformity and distribution to maintain yield across the wafer. The Purion XEmax ultra high energy implanter, described in this paper, was designed to meet the challenges of the evolving CIS market.

The traditional approach to attaining high energies is the use of ions with very high charge state (such as 4+ and beyond). For industrial applications like ion implantation, the use of very high charge state comes with limited available beam currents and shortened ion source lifetime. The use of very high charge states also makes the system susceptible to energetic metals contamination. For example, when implanting As^{4+}, Fe^{3+} ions, if present in the ion source plasma, could be efficiently accelerated on the RF LINAC to possess a magnetic rigidity close enough to As^{4+} to pass through a magnetic energy filter together with As^{4+} ions, reaching a wafer as an energetic metal contaminant.

Axcelis' Purion XEmax ultra high energy ion implanter is designed with Boost™ Technology to address the shortcomings of the traditional approach. Boost Technology enables accelerating Arsenic up to 15 MeV with the use of only up to 3+ charge state at the ion source. This lower extracted charge state gives great benefits in terms of higher beam currents and much longer ion source life. Boost Technology is also a powerful tool to solve the energetic metal contamination problem, the simplest example being avoiding the use of As^{4+} ion from the ion source to prevent Fe^{3+} contamination. Boost technology increases the charge state of the Arsenic ion between acceleration stages. The accompanying change to the magnetic rigidity of the desired Arsenic ion allows energetic metals that passed the first acceleration stage to be filtered out before entering the second stage.

Use of channeling is rapidly becoming very prevalent to gain extra depth in higher energy implantations. Detailed attention was paid in the Purion XEmax beam line design to produce the best beam angle performance. The newly designed S-bend angle corrector produces the best beam parallelism, while retaining flexibility in the parallelism control. Also, great attention was paid in minimizing the angle distribution within the scanned beam, giving unsurpassed degree of channeling performances.

The paper gives the description of Purion XEmax ultra high energy ion implanter and its performances.

Unique features of FLEXion tool for wide band gap and III-V semiconductor devices fabrication

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Wide bandgap and III-V semiconductor devices are recently experiencing an incredible market growth due to their use in new electric and autonomous vehicles, IOTs and 5G applications. These materials, including SiC and GaN for power and high frequency electronics, GaAs, InGaAs, InP, HgCdTe, InAs, InSb and GaSb for RF devices and optoelectronics require specific ion implantation species and conditions for the fabrication of junctions, contact or insolating layers. For example, in SiC, as no diffusion occurs and as implant defects are very difficult to recover, multiple implantations steps of aluminum at above 500°C with different energies, sometime above 1MeV, are required to tailor the desired doping profile for the fabrication of p doped layers. GaN requires the use of Mg implantation, while other compound materials need other “exotic” species as H, He, Fe, Be, In, Cd…As most these susbtrates are available only on smaller than 200 mm wafers, the use of expensive downgraded 300 mm implanters optimized for silicon doping is not technically and economically efficient and old generations of 200 mm tools do not cover all the requirements. To specifically address the new implantation needs of these wide band gap and III-V materials, IBS has developed a new implantation platform, named FLEXion. The flexibility of the tool allows to implant more than 65 species using either an Indirectly Heated Cathode (IHC) or a sputtering source. Secured generation of H^+ beam can be achieved thanks to the use of hydrogen generator from water. High energy implantations are allowed thanks to the 400 kV acceleration capability combined with the possibility to generate multiple charged ions (up to 5+) using a new ECR source. High temperature implant (up to 650°C) as well as cryogenic implantation (down to -100°C) are possible using different chuck options, including a fast ramping heating e-chuck. The optimized auto-tuning system allows easy and quick processing of multistep implantations (up to 10 steps). Its high-resolution spectrometer ($m/\Delta M > 140$) avoids any cross-contamination risks as reported when implanting multiple charged [1] or high mass ions on other competitor tools (fig. 1 & 2).

All these unique characteristics will be presented and applications for various wide band gap and compound devices fabrication will be discussed.

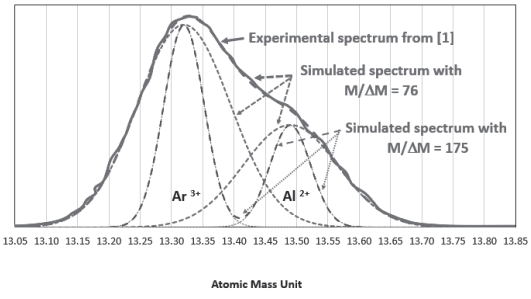

Fig.1 : Illustration of Ar^{3+} contamination on an Al^{2+} implant on a competitor implanter with a mass resolution of about 76 from [1] (red curves), comparison with a simulated mass spectrum with a resolution of 175 for the same recipe (blue curve).

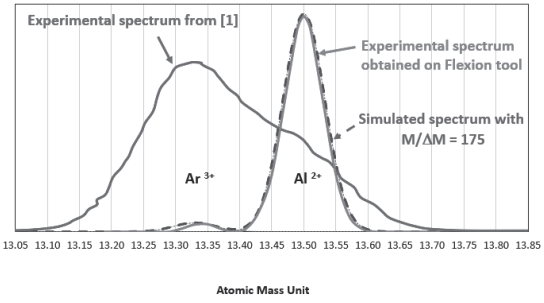

Fig.2 : Comparison with mass spectrum experimentally obtained on FLEXion with a mass resolution of about 175 and an optimized recipe to obtain multicharged Al with reduced Ar contamination

[1] Volker Häublein : Energetic Contamination in Al Implants. European Ion Implantation User group meeting n°59, IISB Erlangen, 12. April 2018

Compositional Measurement of Confined SiGe Devices with Self Focusing SIMS

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The continued downscaling of semiconductor transistors, both laterally and in depth, results in acute characterization challenges. Metrology tools must ensure lateral resolution of a few nanometers as well as high depth resolution while retaining high sensitivity. Dynamic Secondary Ion Mass Spectrometry (SIMS) enables access to high depth resolution at low primary impact energies (≤500 eV). However, it still utilizes a micron sized beam to probe nanometer sized structures. In order to overcome the beam size limitation when analyzing small features, one can seek to localize (laterally and in depth) the signal emitted by the device by specifically tracking the molecular secondary ions emitted from the 3D area of interest. This novel method is referred to as Self-Focusing SIMS [1]. This is possible if 1) there exist mass peaks in the spectra which can be identified as originating only from the 3D device area or layer of interest and 2) the emission of secondary ions from surrounding device area is suppressed or negligibly small. In the case of a SiGe device, one looks for the Ge^{2+} signal while taking all Ge containing molecular ions in the mass spectra into account

Four test samples produced by the same SiGe growth recipe were employed to both investigate a micro-loading growth effect and validate the developed quantification model. The samples used were a SiGe blanket wafer, a SIMS pad in the scribe line (50x60 μm^2) which is larger than the beam size, an equally spaced uniformly boron doped vertical SiGe FIN structure with evenly spaced SiGe and Si_3N_4, and an SRAM device with SiGe structure occupying 11% of the total analysis area.

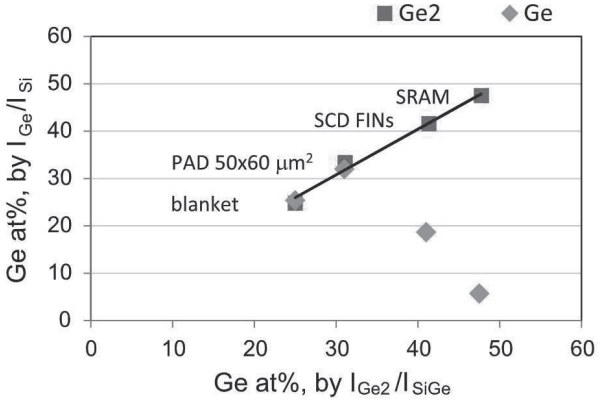

Figure 1:A microloading growth effect is identified by using the Ge clusters in a self-focusing SIMS approach on the confined SiGe structures. In addition, the fraction of analyzed area occupied by the SiGe structures is represented by the degree of underestimation of Ge concentration obtained by conventional SIMS approach, instead of the self-focusing approach.

This approach to analyzing small features is about ten times faster than a direct study of the feature with say TEM or APT. In addition, as SIMS is averaging over many such structures, the signal-to-noise is high, resulting in more statistically reliable results compared to TEM or APT. On the other hand, no compositional variation within the confined area can be determined using this technique.

[1] A. Franquet et al., Appl. Surf. Sci. 365 (2016), 143

Detection of Particles in the Ion Beam

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Particles carried in the beam line during the implantation processing are transported downstream by the ion beam [1, 2], adhere to the wafer, and can act as unintended "masks" and reduce product yield. In batch type implanters, the generation of particles in the beam line and the chamber can be monitored by setting an in-situ particle monitor near the wafer and measuring the particles in the atmosphere of the disk chamber [3]. However, in the single wafer implanters, with lower velocity wafer motions, it is more difficult to implement such direct particle detection systems and provide real-time warning of sudden particle generation.

We are developing a real time particle monitor for the single wafer implanters. This new system consists of a laser beam incident perpendicular to the ion beam and a high-sensitivity camera that detects the scattered light from the particles. There are two major differences from the conventional in-situ particle monitor. First, the particle monitor under development observes the particles present in the ion beam implanted into the wafer, rather than the chamber atmosphere. Second, it obtains the two-dimensional information from the camera and detects the generation of particles by image processing. We conducted an experiment to explore the possibility of this new particle monitoring system. Graphite powder was artificially introduced into the ion beam upstream of the observation region as dummy particles, and video images were captured with the camera during the implantation processing. After the implantation, the number of particles attached to the wafer was measured by a surface inspection device.

In this presentation, we report the method for quantifying the captured particle images in the ion beam by image processing and the correlation with the number of particles on the wafer after implantation processing.

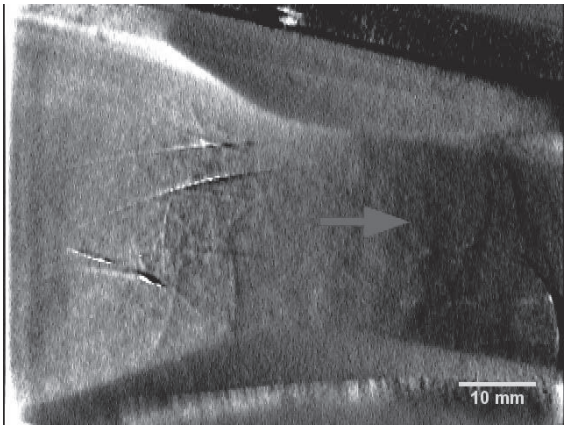

Figure 1. Particles appeared as bright lines on the left side of the image. These lines were observed when an ion beam was emitted. Red arrow indicates the ion beam direction. Note that the contrast has been adjusted to improve clarity.

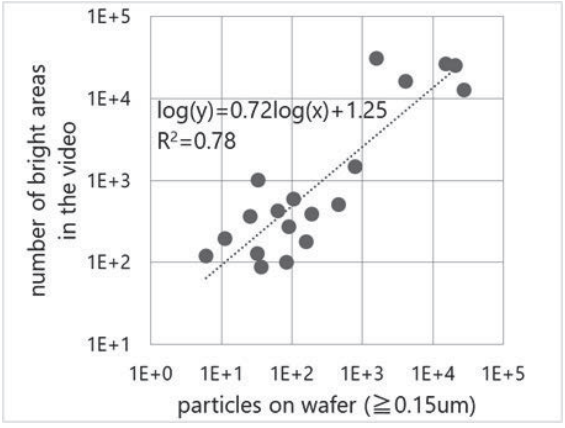

Figure 2. The number of particles on the wafer (horizontal axis) and the value obtained by image processing (vertical axis). Log-log regression is shown by dotted line.

References:

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[2] D.A Brown *et al.*, "On transport and heating of particulate contamination entrapped in an intense cylindrical ion beam," J. Vac. Sci Technol. A9(5), (1991) 2808-2812.

[3] B. Fishkin, M.I. Current, "Method and apparatus for detecting particles in ion implantation machines", US patent, 5,047,648, Sept 10, 1991.

Reduction of Wafer Charging Effects with Advanced Electrostatic Chuck Technologies

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Wafer charging is a challenging issue in the ion implantation process. The implantation of positive ions presents a device risk, which must be managed and mitigated. There are various approaches to resolving wafer charging issues, especially the use of electron floods, to compensate the positive implanted charge. In this work, we examine electrostatic chuck (ESC) technology, advanced ESC features, and ESC operational parameters to evaluate the impact of these variables on wafer charging as determined by SPV measurements.

The requirements of the implant process have driven ESC suppliers to introduce structures into the ESC design to improve ESC behavior in the implant environment [1]. These structures (or features) are principally included to prevent wafer sticking issues, but they provide charge control that also benefits wafer charging. We compare a conventional Johnsen-Rahbek (JR) technology ESC (JR-ESC) to an advanced Coulombic ESC (C-ESC). The C-ESC is advanced in the sense that it includes several features to relax residual charge on the ESC. To evaluate wafer charging, we use the SPV method [2], which measures the light-generated voltage that develops across a thick frontside oxide (100nm) during implant. We find that the advanced C-ESC produces smaller and near-zero SPV response whenever the electron flood is on. The conventional JR-ESC produces an SPV response that basically follows the clamp force, producing a negative SPV response that is increasingly negative as clamp force is increased.

Since an ideal wafer charging response would always be zero, the advanced Coulombic ESC is superior for this response. SPV process limits are often biased towards negative readings due to fear of positive voltage causing damage and here, a parametric response is observed, so optimization can be performed. We will present full characterization of the SPV response of several generations of ESC technology.

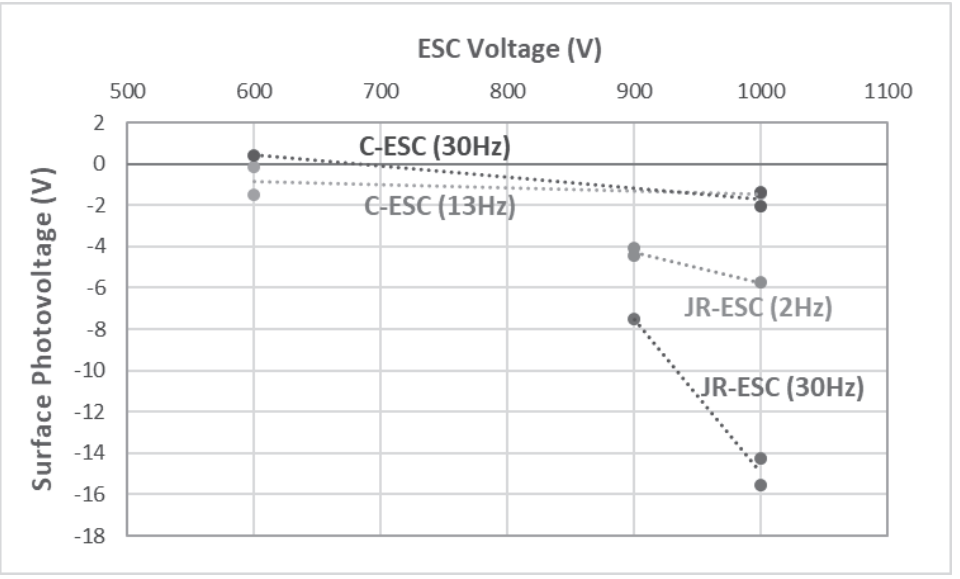

***Figure 1**: Surface Photovoltage (SPV) responses comparing a conventional Johnsen-Rahbek chuck (JR-ESC) with an advanced Coulombic chuck (C-ESC) containing advanced charge dissipation features.*

Sheet-Resistance Measurement for Ultra-High Energy Ion Implantation

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To improve light sensitivity of advanced image sensors with deep photodiode structures, high implant energy is required by ion implanters. To meet these energy requirements, Sumitomo Heavy Industries Ion Technology has released single-wafer ultra-high energy implanters, such as S-UHE [1] and SS-UHE [2], which can realize 3 μm or deeper implantation. Although these tools enable deeper implantation, the conditions near the wafer surface may be different than those at shallow implantation. Therefore, it is not always possible to measure the characteristics of the wafer using conventional diagnostics.

As an example, in Fig. 1, we depict the depth profiles of carrier concentration in the silicon wafers that are implanted using phosphorus at various high energies. The electrical conductivity of the positive-type wafer became negative because of phosphorus implantation with the energies of 1.5, 2, and 3 MeV. However, the surface regions of the 6-MeV implanted wafer were still positive. This means that the phosphorus concentration in the vicinity of the wafer surface was not sufficiently high for the surface to be negative. This is because as the implant energy increases, the dopant ions implant deeper into the wafer. Therefore, the electrical sheet resistance of the wafer cannot be measured using conventional four-point-probe tools. To measure the sheet resistance of such wafers, a sacrificial oxide layer was applied onto the wafer surface and removed after ion implantation.

In Fig. 2, we depict the sheet-resistance map of the wafer-implanted phosphorus with the energy of 6 MeV. The thickness of the sacrificial SiO_2 layer was 1.5 μm, which is considerably thicker than that of the positive-type layer. Because of this method, the sheet resistance can be measured with satisfactory uniformity. In this report, other examples of arsenic implanted with considerably high energy are discussed.

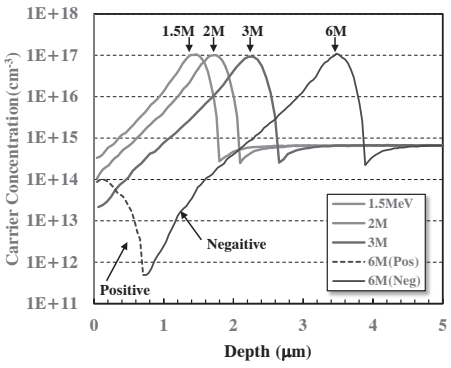
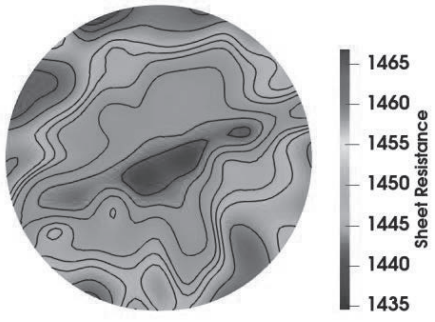


Fig 1. Results of spreading resistance analysis of the silicon wafers implanted using phosphorus with various energies. The surface region of the 6-MeV implanted wafer was still positive-type conductivity since phosphorus concentration was smaller than boron concentration of the substrate.



Average: 1452.5 ohm
Uniformity: 0.427 %

Fig 2. Sheet-resistance map of the wafer implanted using phosphorus (6 MeV, 5E12 /cm^2) through a 1.5-μm SiO_2 layer. The SiO_2 layer was removed via HF etching before the measurement.

References

(1) K. Watanabe *et al*., Ion Implantation Technology 2014 proceedings
(2) https://shi-ion.jp/products/s-uhe-he/, accessed on March 19, 2020

Low Temperature Monitoring with Implantation and Silicidation

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Thermal processes are some of the key processes in semiconductor manufacturing. The temperature-time cycle has changed radically over the past 20 years and the monitoring of manufacturing equipments is of paramount importance for the stability of the manufacturing process. Therefore, various thermal cycles schemes are under investigation to monitor continuously the status of lamp-based production process and equipment in between the manufacturing runs to ensure the best process results and predict early issues with tool or pre-processes.
In general it is becoming obvious in the industry that the thermal processing trend is heading towards extreme directions: on the one hand, the high temperature regime with millisecond processing times for forming optimal junctions and on the other hand, to the very low temperature processing regime with temperatures from room temperature up to 800 °C and durations of up to several seconds for forming high quality silicide layers with minimum consumption of Silicon material and good conformality in case of 3D-structures. This paper examines and present especially the complex monitoring process for low temperature processing by a defined implantation condition capable of monitoring processes below 800 °C as well as a comparison to a special TiAl metal alloying method to ensure the process requirements of the manufacturing flow.

Physical, Electrical and Electrochemical Characterization of 2D Materials (Graphite, GNP and GO)

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The characterization of different materials, specifically carbonaceous materials, requires combinations of different microscopic and spectroscopic techniques. Among the various Spectroscopic techniques widely used for the characterization of 2D materials, electrochemical impedance spectroscopy (EIS) is a robust, simple, non-destructive, and powerful electroanalytical technique that provides a considerable amount of information about kinetics happening inside a battery in a comparatively short period. The spectrum produced due to the EIS measurement gives a couple of important information to the user, such as the reactions occurring in the cathode and anode in separated features. Furthermore, if the time constants are resolvable, EIS provides ample information about the resistance arising from each kinetic step during the electrochemical reaction in the electrodes. Keeping this in mind, this study concerns characterization of three different carbon allotropes (Graphite, GNP and GO) via different spectroscopic techniques such as Raman Spectroscopy and X-ray photoelectron Spectroscopy. These materials were then used in a sodium-ion half-cell setup as cathode material. Afterwards, three different carbon allotropes were examined and differentiated using EIS due to the discrepancy in impedance of electrodes with varying depths of charge/discharge cycles. Furthermore, the study involved the investigation of reaction mechanism and kinetics during sodiation/disodiation. Therefore, it was found that electrochemical performance tests and EIS data can embellish the previously obtained results from the spectroscopic techniques and enhance the understanding of fabricating better anodes for sodium-ion batteries.

Preference for Oral Presentation, Topic: Metrologies for Implant/Doping and Annealing Processes (Physical and Electrical Characterization of 2D and 3D structures), Keywords: EIS, 2D Materials, Characterization

Ion Implantation Simulation and Optimization in Semiconductor Compounds

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An ion implantation simulator called INNOViON coded on MATLAB software and using SRIM (Stopping and Range of Ions in Matter) simulated data is introduced. Using this application, ion and vacancy distributions in a target for multiple implant energies can be generated. In addition, inherent SRIM limitations and mitigation techniques embedded inside INNOViON are discussed. A Monte-Carlo profile matching optimization principle, a very useful feature for isolation ion implantation processing, is discussed. Finally, a heuristic channeling simulation capability based on multiple profiles found in the literature is described.

Since the 1980s, several codes, such as SRIM/TRIM, UT-MARLOWE, COSIPO, ACOCT PEPPER, CrystalTRIM, have been focusing on modeling ion ranges and damage distributions, in terms of created vacancies, in amorphous or crystalline targets. This paper presents a modeling expansion application coded on MATLAB which builds on SRIM simulated data and optimizes its modeling capability and computing speed. It allows for fast and high accuracy design of ion implantation sequences into semiconductor compound targets (Figure 1).

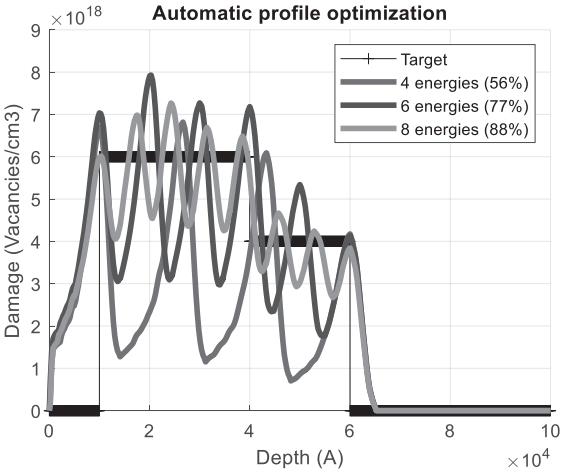

Figure 1. Automatic profile generated for hydrogen implants into an InP substrate with the target profile in thick straight black lines. Increasing the number of energy/dose steps leads to a higher matching ratio, defined as the percentage of one minus the difference between the target and simulated profiles, as listed in the figure.

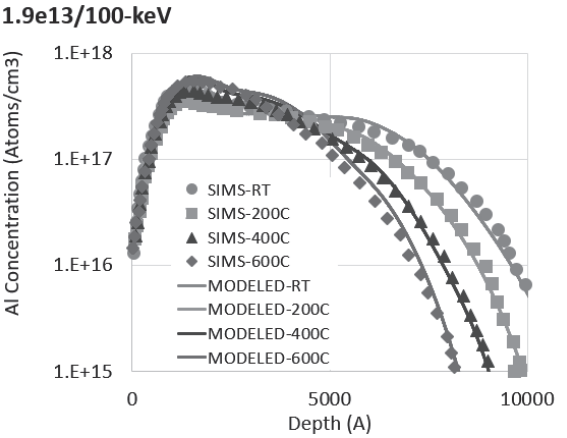

Figure 2. Comparison between SIMS profiles and simulations for Aluminum implants into the 4H-SiC [0001] channel with dependence on temperature.

For SiC applications, since the diffusion of dopants is nearly nonexistent, the channeling effect is often being used to implant a “box profile” into the substrate. We developed a heuristic method based on a Taylor-Young expansion into Gaussian functions of channeled ion curves extracted from Secondary-Ion Mass Spectroscopy (SIMS) profiles found in the literature. By determining the evolution of the Gaussian functions with energy, dose, and temperature the simulator can recreate the channeled curves. See Figure 2 for the case of Aluminum into the [0001] main channel of 4H-SiC and the profile channeling dependence on dose and temperature. This heuristic method enables the simulator to model channeling effect with energy, temperature, and dose, for substrates where diffusion is prevented and to accurately reproduce SIMS experimental results.

Optimization of doped lanthanated tungsten components in ion sources by determining the temperature profile for halogen processes

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Abstract

Aggressive environments like fluorinated source gases lead to erosion and wear (halogen cycle) in ion implant equipment. Lanthanated tungsten (WL) has been commonly used in these applications, primarily in ion implant sources. Especially the process gas GeF_4 produces a large amount of free fluorine radicals. The present work involves the practical and theoretical evaluation of a realistic, in-situ process temperature profile of an ion source equipped with WL liners. Hereby a GeF_4 environment was investigated to confirm the functionality of WL materials at elevated temperatures above 1000°C. The two routes chosen in this work are a practical approach on one hand. An ion source was redesigned to hold up to two modified ceramic sintering tablets (“Temp Tabs”) to produce data sets that are used to define the exposed plasma temperature. On the other hand, a numerical simulation of an ion source was established. Both results are finally compared to create a realistic statement regarding the temperature profile. The aim is to get a deep understanding of the behavior of WL in fluorine-rich plasmas relative to the exposed temperature.

IIT 2022 Abstract

Cryogenic Implantation to Boost PFET Performance and Improve Variability in 3D NAND Flows

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Abstract

3D NAND scaling includes 1) vertically building more pairs and stacking multiple tiers along with ON thickness reduction for each pair, and 2) horizontally scaling the cell (Cell and Array or CnA), or building CMOS under Array (CuA), [similar termed such as Peri under Array (PuA) or Cell over Peri (CoP)]. It is required to boost CMOS FET performance to drive 3D NAND cell by overcoming Short Channel Effect (SCE), Narrow Width Effect (NWE), and dopant deactivation from further thermal processes after peri-CMOS formation. Comparison studies between CuA and CnA showed with higher drive current (I_{DS}), but Vt lowered and degraded Ioff by ~10x for CuA architecture.

It is well established that cryogenic implant can be used to boost device performance by reducing implant induced damage or defects in End of Range (EOR) [1-2]. Controlling interstitials enable to minimize dopants, such as Boron or Phosphorus, Transient Enhanced Diffusion (TED) during subsequent thermal process. Therefore, scaled device Short Channel Effect (SCE) would be minimized and better device performance with reduced variability can be achieved through uniformly formed implant layers. In this paper, we focus on Crion® technology, down to -100°C temperature and carbon co-implant to minimize SCE and off leakage performance of PFET. Device Vt variability improvement is also demonstrated.

Keywords : 3D NAND, Cryogenic implant, Variability control

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Review of Applications of Defect Photoluminescence Imaging (DPLI) to Monitoring Crystallographic Defects during IC Processing

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Keywords; nonvisible defects in IC, defect Photoluminescence in Si, defects during ion implantation

Abstract
The low efficiency of DPL (Defect Photoluminescence) of individual crystallographic defect such as dislocation or stacking faults in Si presents significant challenges to effective imaging and localizing of these individual crystallographic defects in Si at room temperature. Recently automated, IC fab compatible tools have become commercially available which allow to identify and localize crystallographic defects on IC Si wafers at various stages of processing with precision of 1µm of defect localization and inspection speed of few seconds per field of view (FOV) of 2.5E-4 to 2.5E-2 cm^{-2} (depends on used magnification). It captures the DPL image from illuminated area of Si wafer. The individual dislocations, stacking faults or oxygen precipitates appears as bright spots on the analyzed images.
This paper reviews the usage of DPLI (Defect Photoluminescence Imaging) to monitor crystallographic defect formation during IC processing.

Advanced Process Control Method for Inline Isolation Implant Monitoring in III-V GaAs Semiconductor Fabrication

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Abstract:
In this paper a method for accurately monitoring the isolation ion implant process of III-V GaAs devices inline, immediately after implant module and detect when there are process excursions, will be discussed. Current available methods of inline implant monitoring of III-V materials do not give the precision to detect small shifts due to equipment and/or process issues, and the risk increases when there are multiple implant steps. For example, with current methods of inline monitoring an energy shift due to a system mis-calibration may not be detected with standard contactless sheet resistance monitoring techniques available [1], and with the weeks long delay between the implant process and electrical testing, delayed detection of excursions poses a high risk for mass production fabs that require isolation ion implantation. By use of this advanced process control technique, the implant process can be checked inline immediately after implant by utilizing a short loop test structure that goes through all the processing steps of the technology up until the implant process module and mimics the standard implanted HBT base sheet resistance isolation test structure but utilizes metal deposition prior to implant for the test structure pads and interconnects (standard test structure receives metal deposition much later on in process and is not tested until final electrical testing). The method discussed in this paper is specific for the advanced processing control of Helium Ion implantation on GaAs patterned substrate. The inline test was found to have a precision of up to +/-10% in energy and +/-20% dose shift for this certain application, but further improvement in precision may be achievable. It was also found that appropriate post implantation annealing was required to activate the implant for reliable results [2]. Results were repeatable on multiple ion implanters and multiple wafer lots showing that this technique has very good potential and can be expanded upon other technologies and materials such as GaN and InP.

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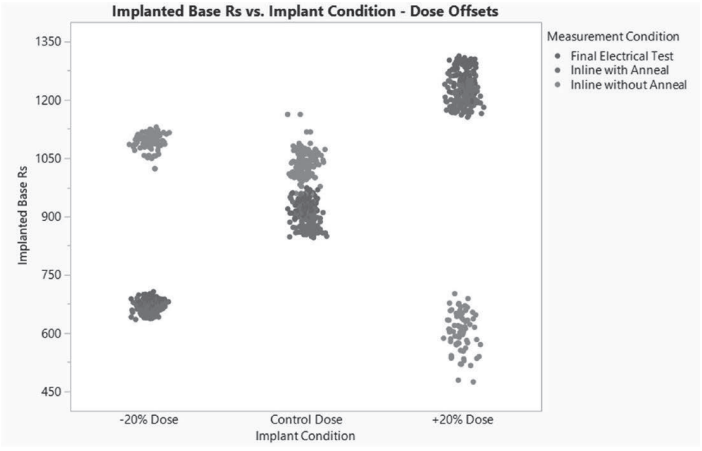

Figure 1: Implanted base sheet resistance plotted by dose variation. Plot is colored by measurement condition to show that inline measurement with annealing lines up with final electrical test.

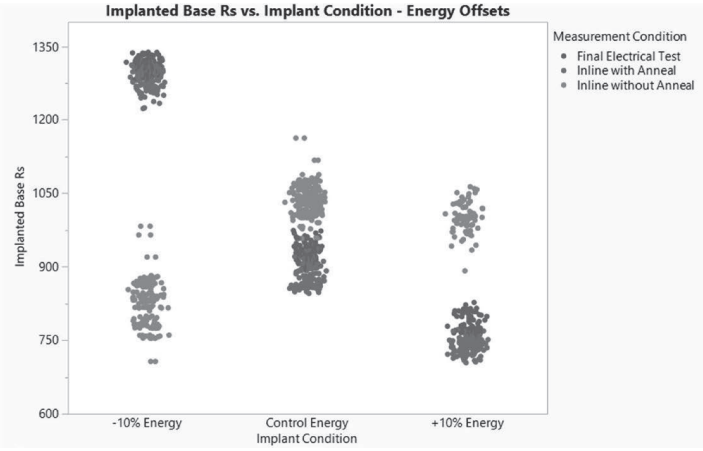

Figure 2: Implanted base sheet resistance plotted by energy variation. Plot is colored by measurement condition to show that inline measurement with annealing lines up with final electrical test.

Defect Microstructure in Ion Implanted GaN

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Nitride compound semiconductors like GaN, AlN or InN are nowadays basis for enormous markets comprising white LEDs, lasers, and high power and high frequency transistors. Ion implantation is the principal technique applied for doping of this type of semiconductors. As a consequence, different defects were created strongly influencing electrical properties of the implanted substrate. Defect properties in GaN have been studied since at least two decades and the state of art can be summarized as follows: self-interstitial and antisite defects have high formation energy in GaN, and thus, are unlikely to occur during crystal growth. These defects may still be created under nonequilibrium conditions, for instance by electron irradiation or ion implantation. Also nitrogen vacancies (V_N) are high-energy defects and it is very unlikely that they would form spontaneously during growth of unintentionally doped GaN. In contrast, the gallium vacancy (V_{Ga}) is the lowest energy defect in n-type GaN. The gallium interstitial produces large lattice relaxations and it can occupy distinct locations in the open spaces of the wurtzite structure. Formation of simple defects results in the stress buildup in the bombarded region, which is the driving force for further defect transformations.

In this study we have applied Molecular Dynamics calculations in order to follow the process of defect formation and their subsequent agglomeration. Fig.1 shows the time dependence of collision cascade produced by 200 keV Ga ion. Number of produced vacancies increases rapidly during the initial stage of the cascade, however, in the cooling phase approx. 65% vacancies recombine with the produced interstitials.

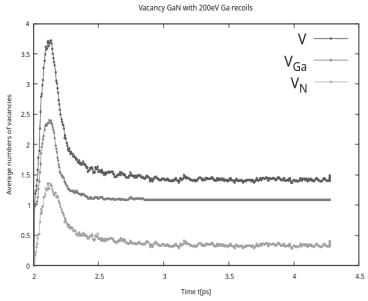

Fig. 1. Time dependence of the number of vacancies produced in the collision cascade. The curve labelled V is the sum of both types of vacancies.

Basing on the energy dependence on number of produced defects the displacement energy for defects in different sublattices was determined. It amounts 47 eV and 109 eV for Ga and N sublattice, respectively. Antisite defects Ga_N and N_{Ga} play crucial role in the semiconductor device physics. We have shown that they are much more stable than other simple defects and are produced at approximately 10 times lower rate than interstitials. Upon prolonged ion bombardment defect clustering occurs. It was noticed that predominantly Ga interstitials agglomerate forming a dumbbell configuration. With increasing ion fluence dumbbells agglomerate forming chaotic extended structures. However, some of these structures arrange in a quasi-hexagonal network reflecting the structure of the native crystal.

Calculated concentration of Ga interstitial clusters was related to experimental data on the stress buildup upon ion bombardment. Reasonable correlation has been observed.

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Silicon Damage from Timescale Modulation for Dose Accumulation in Single Implant and Damage Interactions Between Multiple Implants

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It is generally known that changes in ion beam current can affect damage distributions in silicon as measured by ThermaWave and SIMS, or amorphous layer thickness as measured by TEM. However, these effects are difficult to quantify, because there are several variables involved in determining the rate of dose and damage accumulation. Vacancy/interstitial recombination occurs at implant temperatures on time scales ranging from picoseconds to microseconds. Thus the probability of an incoming ion interacting with an interstitial atom that was recently dislodged from its lattice site (and would have recombined naturally at implant temperature in the absence of the new ion) will depend on the beam density and scan frequencies/duty cycles of the beam.

We varied the accumulation of dose on a scanned spot beam implanter by adjusting horizontal scanning frequency, vertical scanning speed (to break the dose up into multiple passes) and breaking up the dose into multiple implants with variable queue time between implanting portions of the dose. We used a single spot beam tune to decouple various timescales of vacancy/interstitial recombination from variables associated with the properties of the ion beam. Angle and dose rate/relaxation effects on ion channeling are deconvoluted by observing the evolution of the channeling tail with two beam densities at dose levels transitioning through the critical dose for amorphization.

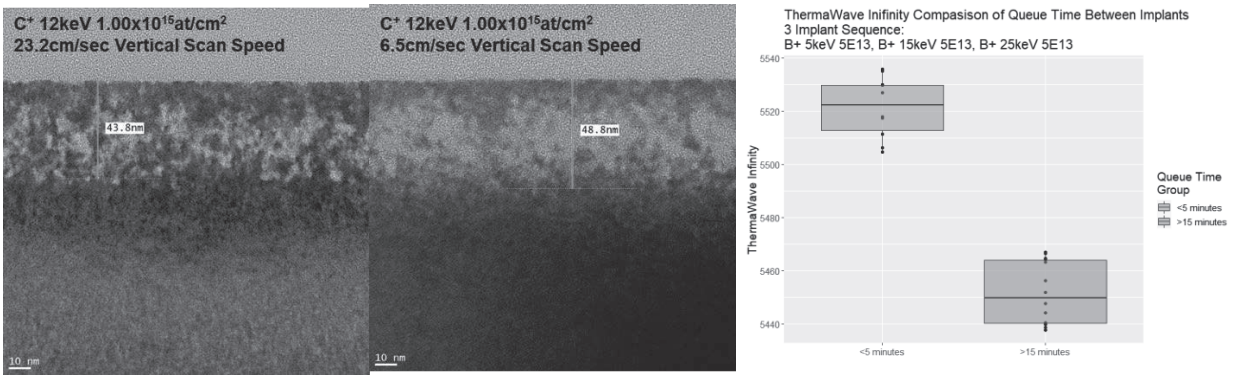

Figure 1: Measured change in Carbon damge layer thickness for the same beam when changing mechanical scanning and changes in ThermaWave Infinity for same sequence of three boron implants by modulating the queue time between implants.

ThermaWave (infinity and decay factors), SIMS channeling profiles, and amorphization as measured by TEM are used to quantify damage differences. The data proves that although the timescale for most of the damage relaxation is short enough that beam current, spot size, scanning frequency and scanning velocity dominate the final damage the continued relaxation is nontrivial. We also prove that the queue time between implants into the same mask can change the final accumulated damage, its effect on dopant placement, and characteristics of the amorphous layers.

Defects and Dopants Behavior of Medium Dose Range Implant into Heated Silicon Wafers

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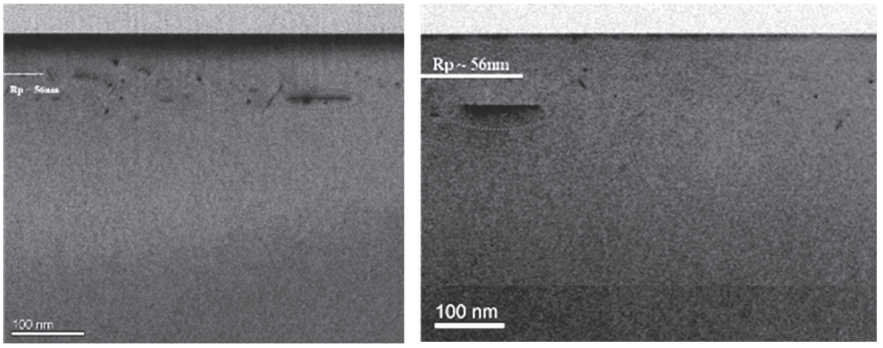
The defects behavior of medium dose (~1E14 ions/cm^2) implant had been investigated a long time ago with the high energy implant in many laboratories [1,2]. However, most of the defect studies had focused on the high dose implant and the defects of medium dose implant had been out of focus for a long time. Recently, because the well implant dose has become higher for the better isolation between wells, the 2ndary defects generated by the medium dose implant have been focused by many device manufacturers. In addition, the heated wafer implant, so-called, hot implant, has been applied to minimize the lattice defects at the medium dose range implant.

In this study, the defects behavior of medium dose and relatively low energy implant was investigated. The 2ndary defects could be observed by XTEM analysis at P 50keV and the type of defect was strongly related to the dose, as confirmed in previous studies [1,2]. Meanwhile, the effect of wafer temperature during implant was also investigated in defects and dopant profile point of view. As is well known, the defect density was decreased by increasing the implant temperature for P 50keV [Fig.1]. Regarding the dopant profile, it was getting deeper by the high temperature implant from the as-implanted state even in off channeling (7deg. Tilt & 23deg. Twist) implant [3]. To understand the difference in the dopant behavior, a full range pre-amorphization test was performed. In addition, the species (P vs. B) dependency was also investigated.



(a) (b)

Fig.1. XTEM Images of 2ndary Defects (a) RT Implant, (b) 200degC Implant.

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Metal/Semiconductor Contact Investigations for Applications in Advanced CMOS Technology

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As a result of extreme downscaling, the source/drain of advanced CMOS transistors have limited contact area. The small contact area causes high contact resistances, which make a significant parasitic resistance component for nanoscale CMOS transistors. To guarantee high performance of advanced transistors, ultralow contact resistivity ρ_c in the order of 10^{-10}-10^{-9} $\Omega\cdot cm^2$ is required in the advanced 10 nm CMOS technology and beyond. In this talk, we will review our contact research progress that is relevant to advanced CMOS technologies.

To achieve rigorous ρ_c studies, the ultralow ρ_c of interests demand ultrahigh accuracy of test structures. Therefore we propose a novel multiring circular transmission line model (MR-CTLM) for accurate measurement of ρ_c of 10^{-10}-10^{-9} $\Omega\cdot cm^2$ [1]. The metal resistance induced ρ_c error is substantially suppressed with the MR-CTLM by its multiring configuration.

Using the accurate MR-CTLM test structures, we investigate experimentally multiple contact solutions. We evaluate metal-insulator-semiconductor (MIS) contacts [2] and compare La to Ti contacts on n-Si [3]. We conclude from these two experiments that low Schottky barrier heights contribute to low ρ_c only on lowly or moderately doped semiconductors, but not on highly doped semiconductors.

Next, we mainly focus on Ti or Ti alloy contacts for both n^+-Si and p^+-SiGe. We propose three Ti (germano-)silicidation techniques that utilize (1) pre-contact amorphization implantation (PCAI) [4],[5] (2) Ti-Si co-deposition [5],[6] and (3) atomic layer deposited (ALD) Ti, respectively [7]. With these processes, we demonstrate Ti (germano-)silicides with ultralow ρ_c of $(1\text{-}4)\times10^{-9}$ $\Omega\cdot cm^2$ on both n^+-Si and p^+-SiGe, which meet the ρ_c requirement of 7 nm/5 nm CMOS technology. On p^+-SiGe, we further demonstrate sub-10^{-9} $\Omega\cdot cm^2$ ρ_c with Ga doping, nanosecond laser activation, and Ti contacts [8], [9].

Lastly, we briefly discuss Ge and n-IIIV contacts. The low donor activation and high ρ_c are still major obstacles that prevent the n-Ge and n-IIIV from applications in advanced CMOS technology.

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Strain Characterization of Si+Ge, SiGe+Ge, SiGe+C, Ge+C, Ge+Sn & Si+Ge+Sn Thin Layers Formed By Implantation With RTA or Laser Melt Annealing Using SIMS, XPS, EDX-TEM, Raman and XRD Analysis

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Shota Komago, Ryo Yokogawa, Kazutoshi Yoshioka, Naomi Sawamoto and Atsushi Ogura, Meiji University, Kawasaki, Japan
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We investigated the strain effects of Ge, Sn and C implantation into Si-Cz, Ge-Cz, 45%-SiGe epilayers and 100%-Ge epilayers followed by RTA or laser melt annealing to form surface thin layers of SiGe, SiGeSn, SiGeC, GeSn and GeC. We used multiple cross characterization techniques for chemical concentration including SIMS, XPS and EDX-TEM while XRD and Raman analysis was used for chemical composition and strain. Results for the Si+Ge+Sn implantation before annealing are shown in Fig.1. A 22.5nm surface double amorphous layer is detected by X-TEM and EDX-TEM mapping shows 25%-Ge 15nm thick amorphous layer with 6.3%-Sn while XPS shows 48%-Ge and 7%-Sn. After 1.8J laser melt anneal the surface 22.5nm layer is now single crystal but defective as shown by X-TEM in Fig.2. The 22.5nm melt depth reduces Si content to 80% by EDX-TEM and increases Ge content to 17% with a surface peak of 37%. Sn surface peak is 17% with a melt bulk region level of 2.3%. XPS shows Ge surface peak of 43% and Sn surface peak of 15% with a melt depth of ~25nm. Fig.3 compares after RTA and laser anneal Ge and Sn XPS profiles and content. The 950°C RTA anneal results in a box-like Ge content of 30% with 6%-Sn. XRD results are shown in Fig.4 comparing 950°C RTA to 1.8J laser melt anneals showing the Si (004) peak at 69.1 degree, SiGe (004) peak at 68.4 degree. With RTA, the β-Sn (101) triple peak starts at 32.0 degree and laser melt β-Sn (200) double peak starts at 30.6 degree. Raman results in Fig.5 shows the Si 520cm^{-1} peak. Laser melt anneal shows the second 514cm^{-1} peak corresponding to 15%-Ge or 10%-Sn. RTA anneal shows a second 504cm^{-1} peak corresponding to 40%-Ge or 20%-Sn and third 410cm^{-1} peak corresponding to 100%-Ge or 50%-Sn. Strain evaluation by Raman shows 0.54% compressive strain for the 1.8J laser melt anneal and 1.80% compressive strain for the 950°C RTA anneal.

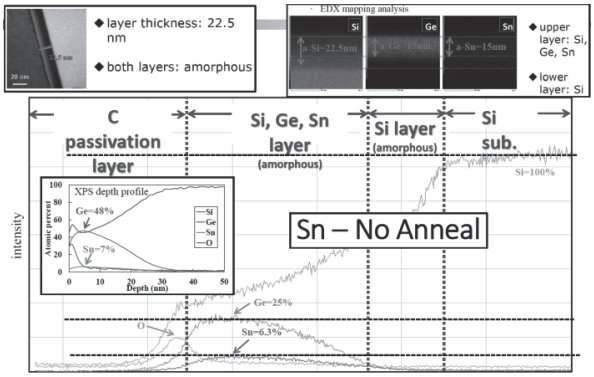

Fig.1: EDX-TEM and XPS analysis of SiGe+Sn implantation no anneal.

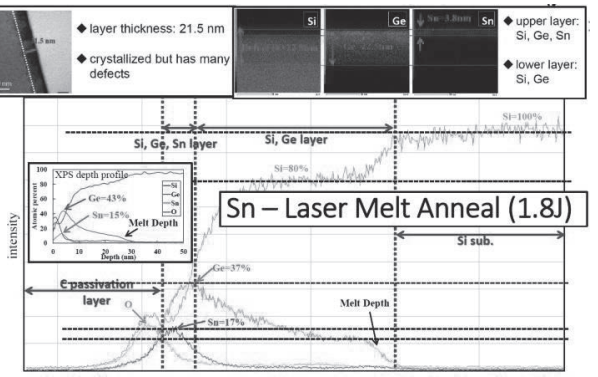

Fig.2: EDX-TEM and XPS analysis after 1.8J laser melt anneal.

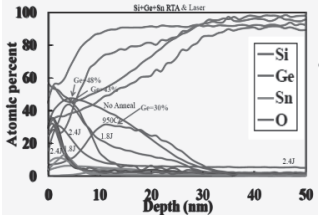

Fig.3: XPS after RTA and melt laser anneal.

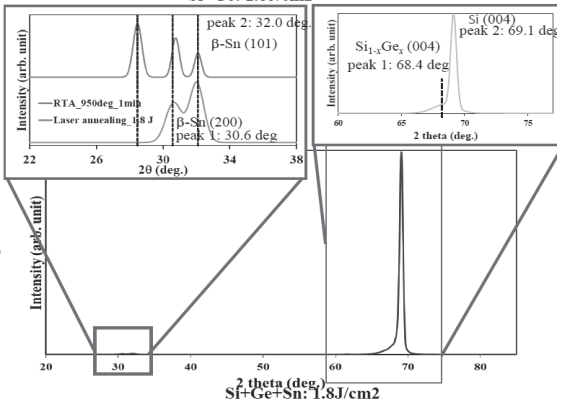

Fig.4: XRD analysis after RTA and melt laser anneal.

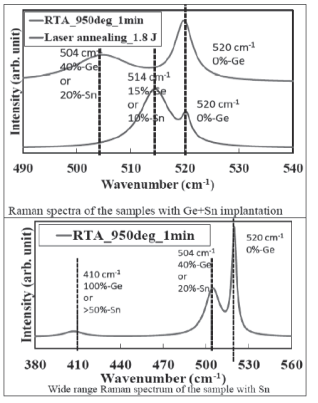

Fig.5: Raman Spectra analysis.

Nitride Stress Inversion Using Plasma Immersion Ion Implantation

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A few decades ago, strain engineering was introduced to improve the mobility of charge carriers in the channel of Metal Oxide Field Effect Transistors (MOSFET) [1]. One method consists in using Contact Etch Stop Layers (CESL) as stress liners. In order to improve both n-MOS and p-MOS performance, the use of a dual stressed liner (DSL) integration is required to obtain two films of opposite stress on the same wafer [2] at the expense of an increased integration complexity. A solution to simplify the DSL integration consists in locally transforming the tensile CESL nitride into a compressive one by ion implantation. As low energy and high fluencies are required for such material modification, Plasma Immersion Ion Implantation (PIII) is well suited for such an application.

For this study, PIII were performed on 300mm silicon wafers capped with 35nm thick tensile PECVD nitride films using a Pulsion® tool manufactured by IBS. Various species (Helium (He), Nitrogen (N), Xenon (Xe) and Argon (Ar)) implanted at various acceleration voltages and doses, adapted to each species, were studied.

The stress of the various nitride layers was determined by the Stoney formula, using curvature measurements and the layer thickness determined by spectroscopic ellipsometry. For all species studied, the PIII process was able to change the nitride stress from initially tensile to neutral or even compressive by increasing the dose and the acceleration voltage (Fig.1). Nitrogen appeared to be the most efficient species to modify the nitride stress without etching the nitride. Indeed, for the other species, tests performed with higher doses than those reported in Fig. 1, to further modify the nitride stress level, led to a layer consumption. Compared to neutral species, the higher efficiency of nitrogen might be explained by its interactions with the damaged nitride layer, resulting in the formation of new chemical bonds and preventing its exodiffusion.

We thus demonstrated the capability of PIII processes to invert the stress of a tensile CESL nitride in a reasonable processing time thanks to the high beam current achievable with PIII. Thanks to these encouraging results, the most promising conditions have been experimented on electrical structures to quantify the static performance gains.

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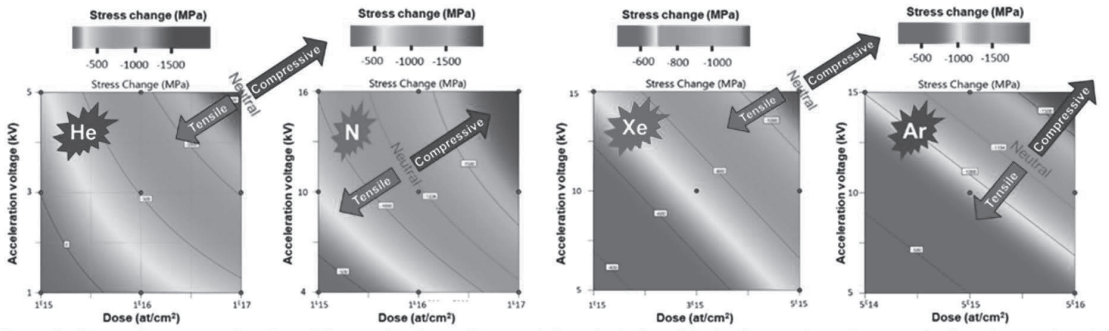

Figure 1 : Stress change as a function of the acceleration voltage and dose for helium (blue), nitrogen (green), xenon (red) and argon (purple)

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[2] Y. Song et al., "Mobility enhancement technology for scaling of CMOS devices: overview and status", 2011 J. of Electronic Materials, vol.40, p1584, 2011.

Key Physical Features and Applications of High Energy Ion Implantation Using the Energy-Filter Technology

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For modern vertical Silicon-Carbide (SiC) power devices accurate custom-tailored doping of voltage sustaining layers is a key issue with respect to device performance and chip cost. Conventional epitaxial doping suffers from large doping variations of up to 20% for nitrogen [1], which entails cost-performance issues, imposes limitations for optimization and complicates wafer diameter scaling. Advanced device concepts, such as superjunction-MOSFETs, are only feasible by applying suitable ion implantation techniques for drift-layer doping. We have developed the so-called “Energy-filter” [2,3 technology, which is based on micropatterned thin membranes which act as degraders for ion beams in the energy range of e.g., 15-24 MeV. This way a monoenergetic beam is transformed into a beam with a well-defined energy range suitable for fabrication of e.g. deep box profiles for nitrogen in SiC, see Fig. 1.

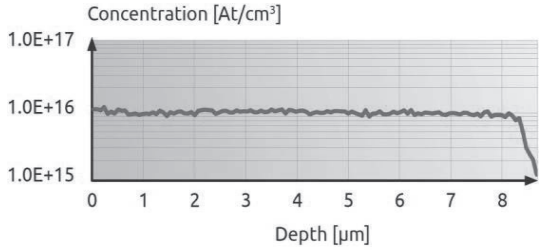

Fig. 1: SIMS profile of 19MeV N-energy-filtered implantation in Silicon-Carbide

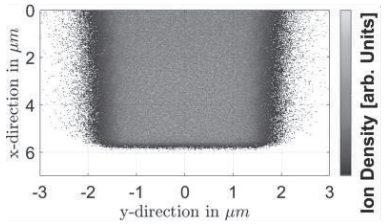

Fig. 2: Geant4 simulation of a 2D-dopant profile of masked energy-filtered implant; 21MeV Al in SiC.

The Energy-filter technology is suitable for manufacturing highly precise (<3%), deep (up to 10µm) and custom-tailored (box, decreasing, increasing) Al or N doping profiles for applications in SiC power devices. In our paper, we will report on various aspects of the Energy-filter technology from fundamental to application aspects.
Energy-filter technology today is available for wafer diameters up to 300mm. A major concern of using thin membranes for energy manipulation is the life-time of these filters. In our experiments we found that several hundred wafers per filter may be processed, without filter degradation. Expected throughputs for typical application cases are above 60 wafers (6”) per hour. CV measurements prove excellent doping homogeneity (<3%). The CV data is supported by electrical chip data comparing conventionally fabricated 650V MPS diodes with energy-filter ion implanted diodes. Besides these more application related aspects, we will show experimental and Monte-Carlo simulation data made by Geant4 [4] on the effects of altered angular distribution for transmitted ion beams. The paper will include a discussion on formation of p-type pillar-like structures, which form the basis for fabrication of superjunction-MOSFETs, see Fig. 2. We will also give an outlook on further applications, in particular novel SiC epitaxial-free engineered substrates and field-stop structures in Silicon-IGBTs.

[1] Wolfspeed materials catalogue, https://assets.wolfspeed.com/uploads/2020/12/materials_catalog.pdf
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